FS8610 – MCU-Based Network Controller with Hardware TCP/IP Protocol Engine

Data Sheet

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Contents

1. General Descriptions

FS8610 is a high performance, MCU-based network controller with Hardware TCP/IP Protocol Engine embedded. Hardware TCP/IP Protocol Engine implements ARP, RARP, IPv4, ICMP, IGMPv2, UDP and TCP protocols, which are all implemented by hardware, to greatly offload MCU's computing power. Not only Software TCP/IP protocol stacks can be totally replaced by Hardware TCP/IP Protocol Engine for program code size saving and for system development more quickly, but also a high network performance can be easily achieved by Hardware TCP/IP Protocol Engine.

High performance 1T Pipelined RISC MCU which is 10 times faster than standard 8051 is embedded in FS8610. MCU clock is dynamically configurable from 25MHz to 160MHz. External SRAM Data memory is extendable to 12M bytes. External Flash/ROM Program memory is up to 2M bytes by hardware-based Code Bank switching mechanism. Program codes can be On-line Updated through network from remote station. FS8610 supports Program Shadow RAM function to greatly enhance program running speed. One high performance DMA is embedded to enhance efficiency of bulk data movement.

FS8610 supports 10BAST-T and 100BAST-TX compilant with IEEE 802.3 and IEEE 802.3u. FS8610 can operates at full duplex or half duplex mode at 10M/100M speed and supports MAC flow control compliant with IEEE 802.3x. Both of VLAN-tagged frame and un-tagged frame are supported.

FS8610 supports 4 independent hardware TCP/UDP socket channels for high performance requirement. It also supports software TCP/UDP socket channels for low data throughput requirement and no socket channel counts are limited. FS8610 also supportes PPPoE connection over xDSL.

FS8610 supports one high speed programmable Sync/Async UART interface from 1200 bps to 230400 bps. 32 high speed GPIO interface are supported not only for general purpose usage but also for I^2C (Master/Slave), I^2S and SPI interface emulation. FS8610 supports expansion SRAM interface to connect with three external applications easily. Three external interrupts are also supported for application uasge.

FS8610 supports Standby mode and Shut Down mode to save power consumption. System can be resumed from Standby mode by Magic packet, Ethernet Link Status Change or External interrupts.

P-Port ICE debug interface, which is connected with FameG D!T-51 tool, makes software development and debugging more easily and efficiency. It helps to reduce system development time and let product at market more soon.

A 25MHz crysal or oscillator is reuired for internal PLL to generate a dynamically programmable system clock. FS8610 is 0.18um process and packaged as 128-pin LQFP. Two external voltage sources 1.8V and 3.3V are required.

2. Features

- Support E8051D with Pipelined RISC 10 times faster standard 8051
- Support dynamic configurable system bus clock from 25MHz to 160MHz
- Support external SRAM main data memory to 2MB, extendable to 12MB (Max.)
- Support external Flash/ROM program memory up to 2MB (32 code banks) with hardware-based Code Bank Switching
- Support Program Shadow RAM function to run program codes from external program SRAM memory instead from external Flash/ROM memory
- Support On-Line Firmware Update function and System Re-initialization from remote station at Program Shadow RAM Enable mode
- Support DMA function for fast and bulk data transfer up to 64KB for each data transfer
- Support MII interface compliant with IEEE 802.3 100BASE-TX and 10BASE-T
- Support Full duplex and Half duplex mode
- Support MAC Flow Control compliant with IEEE 802.3x
- Support flexible MAC multicast address hash filtering
- Support Ethernet frame and IEEE 802.3 frame
- Support VLAN-tagged frame compliant with IEEE 802.3ac
- Support 1 programmable VLAN ID
- Support Hardware ARP/RARP/IPv4/ICMP/IGMPv2/TCP/UDP Protocol Engine without Software TCP/IP protocol stacks
- Support 4 independent hardware TCP/UDP socket channels for high performance requirement
- Support software TCP/UDP socket channels without channel counts limitation
- Support PPPoE connection over xDSL
- Support one high speed programmable Sync/Async UART interface from 1200 bps to 230400 bps
- Support 32 high speed GPIOs interface, which can be emulated such as I^2C (Master/Slave), I^2S and SPI interfaces
- Support Timer 0 and Timer 1 interface
- Support 3 external applications connected at external SRAM data memory interface
- Support 3 external interrupt sources
- Support independent programmable memory bus Read/Write Wait States for Program/Data memory and 3 External applications
- Support Standby mode and Shut Down mode to save power consumption
- Support System Resume from Standby mode by Magic packet, Ethernet Link Status Change or External interrupts
- Support P-Port ICE debug interface
- 128-pin LQFP package

3. Pin Description

3.1. Ethernet MII Interface Signals

Signal Name	Pin No	I/O	Description
TXCLK	**90**	**I**	**Transmit Clock.** TXCLK is a continuous clock from external PHY device. During 100Mbps mode, TXCLK is 25MHz. During 10Mbps mode, TXCLK is 2.5MHz.
TXEN	**95**	**O**	**Transmit Enable** It indicates TXD contains valid data to be transmitted to the external PHY. This signal is synchronous to TXCLK.
TXD[3:0]	**94 ~ 91**	**O**	**Transmit Data [3:0]** This is a group of 4 data signals, which are driven synchronous to TXCLK for transmission to the external PHY. TXD3 is the most significant bit and TXD0 is the least significant bit.
RXCLK	**87**	**I**	**Receive Clock.** RXCLK is a continuous clock from external PHY device. During 100Mbps mode, RXCLK is 25MHz. During 10Mbps mode, RXCLK is 2.5MHz
RXER	**81**	**I**	**Receive Error** It indicates a media error is detected from external PHY.
RXDV	**82**	**I**	**Receive Data Valid** It indicates the recovered and decoded RXD from an external PHY is valid and synchronous to RXCLK.
RXD[3:0]	**86 ~ 83**	**I**	**Receive Data [3:0]** This is a group of 4 signals, sourced from an external PHY that contains data aligned on nibble boundaries and driven synchronous to the RXCLK. RXD3 is the most significant bit and RXD0 is the least significant bit.
COL	**96**	**I**	**Collision Detection** It indicates a collision detected on the media by the external PHY.
CRS	**80**	**I**	**Carrier Sense** It indicates there is a non-idle media by the external PHY.
MDC	**79**	**O**	**Management Data Clock**

			This is a continuous clock to PHY's management interface for management data transfer.
MDIO	**78**	**I/O**	**Management Data Input/Output** This pin is used to transmit or receive management information to PHY.
PHY_RSTB	**97**	**O**	**PHY Reset** When asserted low, it is used to reset external PHY from FS8610.

3.2. External Program/Data Memory Interface Signals

<table>
<tr><th>Signal Name</th><th>Pin No</th><th>I/O</th><th>Description</th></tr>
<tr><td>XADDR[18:0]</td><td>32 ~ 26,
22 ~ 11</td><td>O</td><td>Program/Data Address Bus[18:0]
These pins indicate the lower 19-bit external program/data memory address bus [18:0] pins.</td></tr>
<tr><td>XADDR[23:19]/
Code_Bank[4:0]
{Jumper Setting}</td><td>37 ~ 33</td><td>I/O</td><td>Program/Data Address Bus[23:19]/
Code Bank Number[4:0] {Jumper Setting}
During Power-on reset, this pin is set to input pins and latched for Code Bank jumper setting.
<table>
<tr><td></td><td>Code Bank [4:0]</td><td>Code Bank No.</td></tr>
<tr><td rowspan="4">Program Shadow RAM Enable</td><td>5’d0</td><td>1</td></tr>
<tr><td>5’d1</td><td>2</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>5’d31</td><td>32</td></tr>
<tr><td>Program Shadow RAM Disable</td><td>Fixed to 5’d31</td><td>x</td></tr>
</table>
Note: 0 => Pull Down; 1 => Pull Up
After power-on reset, these pins are set output pins and used as address bus [23:19].</td></tr>
<tr><td>XDATA[7:0]</td><td>8 ~ 1</td><td>I/O</td><td>Program/Data Memory Bus[7:0]
These pins indicate the 8-bit program/data memory bus.</td></tr>
<tr><td>DATA_CSB0</td><td>121</td><td>O</td><td>Main Data Memory Chip Select 0
Active low. This pin indicates external SRAM data memory is selected for read/write access. The address of DATA_CSB0 is fixed in the range from 24’h00_8000 to 24’h20_7FFF.</td></tr>
<tr><td>EXT_CSB1</td><td>120</td><td>O</td><td>External Chip Select 1
Active low. This pin indicates external SRAM data memory is</td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td>selected for read/write accessed. The address is programmable in the range from 24’h20_8000 to 24’hBF_FFFF.</td></tr>
<tr><td>EXT_CSB2</td><td>119</td><td>O</td><td>External Chip Select 2
Active low. This pin indicates external SRAM data memory is selected for read/write accessed. The address is programmable in the range from 24’h20_8000 to 24’hBF_FFFF.</td></tr>
<tr><td>EXT_CSB3/
PRG_CSB</td><td>118</td><td>O</td><td>External Chip Select 3/
Program Memory Chip Select
This pin can be used as External Chip Select 3 signal or Program Memory Chip Select signal depending on Shadow RAM function enabled or not.
<table>
<tr><td></td><td>One
Code Bank</td><td>Multiple
Code Banks</td></tr>
<tr><td>Program Shadow RAM Enable</td><td>EXT_CSB3</td><td>PRG_CSB</td></tr>
<tr><td>Program Shadow RAM Disable</td><td>PRG_CSB</td><td>PRG_CSB</td></tr>
</table>
<u>EXT_CSB3:</u>
Active low. This pin indicates external SRAM data memory is selected for read/write accessed. The address is programmable in the range from 24’h20_8000 to 24’hBF_FFFF.
<u>PRG_CSB:</u>
Active low. This pin indicates external Program memory is selected for read/write access.</td></tr>
<tr><td>DATA_WRB</td><td>123</td><td>O</td><td>Data Memory Write Enable
Active low. This pin indicates external SRAM data memory is selected for write access.</td></tr>
<tr><td>DATA_OEB</td><td>122</td><td>O</td><td>Data Memory Output Enable
Active low. This pin indicates external SRAM data memory is selected for read access.</td></tr>
<tr><td>FLASH_CSB</td><td>126</td><td>O</td><td>Flash Memory Chip Select
This pin can be used as Flash/ROM Memory Chip Select signal at Program Shadow RAM Enable mode or undefined at Program Shadow RAM Disable mode.
<table>
<tr><td></td><td>Definition</td></tr>
<tr><td>Program Shadow RAM Enable</td><td>FLASH_CSB</td></tr>
<tr><td>Program Shadow RAM Disable</td><td>Undefined</td></tr>
</table></td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td>Active low. This pin indicates external Flash memory is selected for read/write access at Program Shadow RAM Enable mode.</td></tr>
<tr><td>FLASH_WRB/
Shadow_En
{Jumper Setting}</td><td>128</td><td>I/O</td><td>Flash Memory Write Enable/
Program Shadow RAM Enable {Jumper Setting}
During Power-on reset, this pin is set to input pins and latched for Program Shadow RAM function jumper setting.
<table><tr><td>Pull Up</td><td>Program Shadow RAM Enable
All of the program codes are copied from Flash memory to Program SRAM memory to run.</td></tr><tr><td>Pull Low</td><td>Program Shadow RAM Disable
All of the program codes are directly run at Flash memory.</td></tr></table>
Active low. After power-on reset, this pin indicates external Flash memory is selected for write access.</td></tr>
<tr><td>FLASH_OEB/
INT_CLK_En
{Jumper Setting}</td><td>127</td><td>I/O</td><td>Flash Memory Read Enable/
Internal Clock Enable {Jumper Setting}
During Power-on reset, this pin is set to input pins and latched for system clock source selection jumper setting. This pin must be pulled up at normal mode.
<table><tr><td>Pull Up</td><td>PLL Mode
Internal PLL clock source is used as system clock for Normal Mode.</td></tr><tr><td>Pull Low</td><td>Bypass Mode
External XI clock source is used as system clock for testing only.</td></tr></table>
Active low. After power-on reset, this pin indicates Flash memory is selected for read access.</td></tr>
</table>

3.3. System Signals

Signal Name	Pin No	I/O	Description
XI	**106**	**I**	**Crystal/Oscillator Input** This pin is used for internal PLL to generate programmable

			system clock. The clock frequency is fixed to 25MHz.
XO	**105**	**O**	**Crystal Output** This pin is used for internal PLL for generating programmable system clock.
PWR_RSTB	**104**	**I**	**Power-on Hardware Reset** Active low. When asserted, FS8610 will be reset.
OP_MD[1:0]	**111, 110**	**I/PD**	**Operation Mode** These pins are used to configure FS8610 into which mode to operate. These pins must be floating and set to Normal mode. 2'b00: Normal Mode Others: Reserved for testing
SCAN_EN	**101**	**I/PD**	**Scan Mode** This pin is used for testing. When FS8610 is configured to Normal Mode, this pin must be gloating and set to Scan Disabled mode. 1: Scan Enable 0: Scan Disable

3.4. UART Interface Signals

Signal Name	Pin No	I/O	Description
UART_TXD	**112**	**O**	**UART Transmit Data** This pin is used as UART transmit data signal.
UART_RXD	**113**	**I/O/ PU**	**UART Receive Data** This pin is used as UART receive data signal.

3.5. Timer Interface Signals

Signal Name	Pin No	I/O	Description
Timer0_CLK	**115**	**I/PD**	**Timer 0 Clock Input** This pin is used as clock input of Timer 0.
Timer0_Gate	**114**	**I/PD**	**Timer 0 Gate** Active high. This pin is used as Gate input of Timer 0.
Timer1_CLK	**117**	**I/PD**	**Timer 1 Clock Input** This pin is used as clock input of Timer 1.
Timer1_Gate	**116**	**I/PD**	**Timer 1 Gate** Active high. This pin is used as Gate input of Timer 1.

3.6. GPIO Interface Signals

Signal Name	Pin No	I/O	Description
GPIO0[7:0]	**47 ~ 40**	**I/O/ PU**	**General Purpose Input/Output Group 0[7:0]** GPIO group 0 pins can be used as input or output pins for general purpose.
GPIO1[7:0]	**54 ~ 48, 58**	**I/O/ PU**	**General Purpose Input/Output Group 1]7:0]** GPIO group 1 pins can be used as input or output pins for general purpose.
GPIO2[7:0]	**66 ~ 59**	**I/O/ PU**	**General Purpose Input/Output Group 2[7:0]** GPIO group 2 pins can be used as input or output pins for general purpose.
GPIO3[7:3]	**77 ~ 76, 72 ~ 70**	**I/O/ PU**	**General Purpose Input/Output Group 3[7:3]** GPIO group 3 pins[7:3] can be used as input or output pins for general purpose.
GPIO3[2:0]/ EXT_INTB[2:0]	**69 ~ 67**	**I/O/ PU**	**General Purpose Input/Output Group 3[2:0]/ EXT_INTB[2:0]** GPIO group 3 pins[2:0] can be used as input or output pins for general purpose or used as External Interrupt Sources [2:0] inputs. While used as External Interrupt source, the signal is active low.

3.7. P-Port Debug Interface Signals

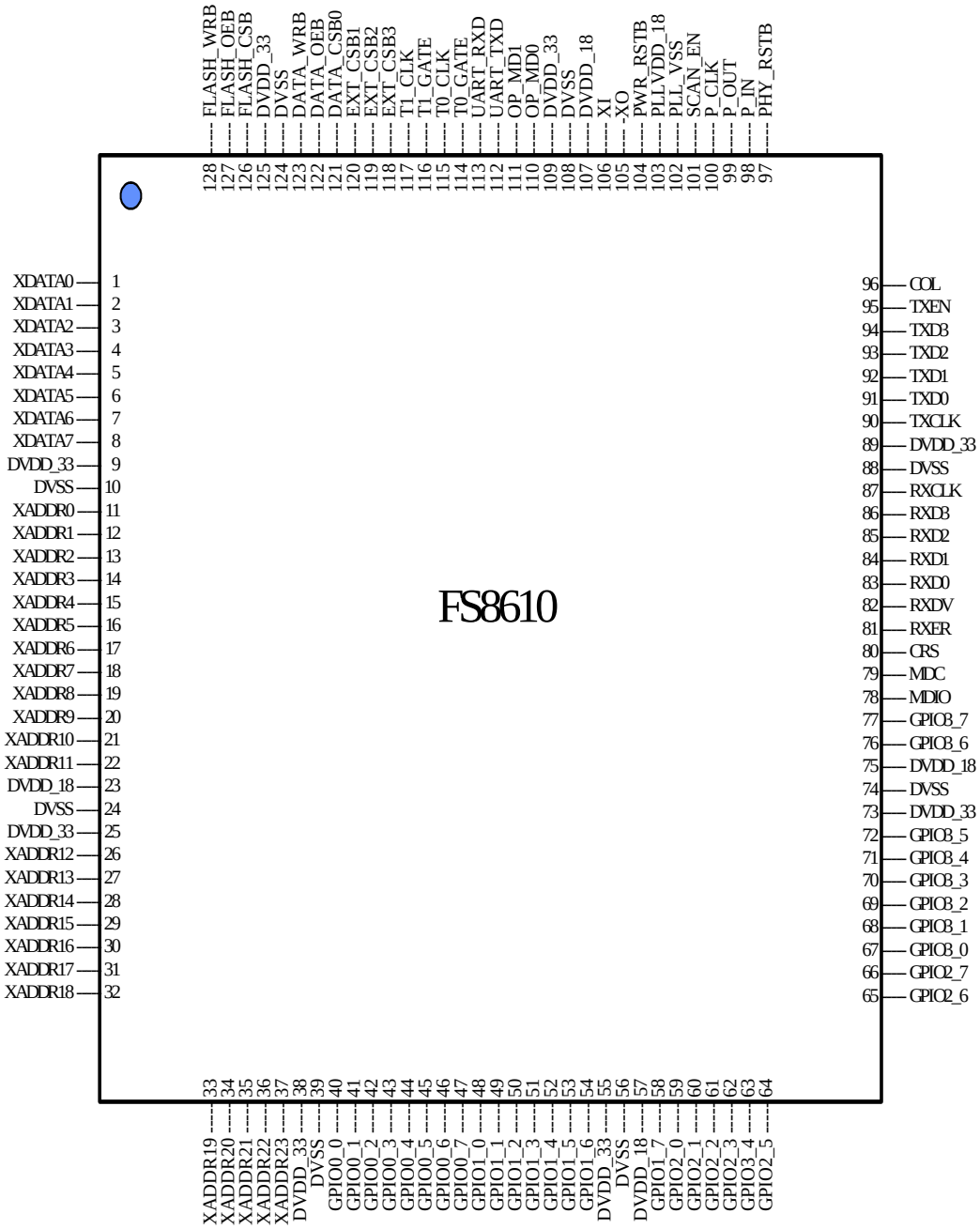
Signal Name	Pin No	I/O	Description
P_CLK	**100**	**O**	**P-Port Clock** This signal is used as P-Port clock input for D!T-51 ICE debugger.
P_IN	**98**	**I/PU**	**P-Port Data Input** This pin is used as P-Port Data input for D!T-51 ICE debugger.
P_OUT	**99**	**O**	**P-Port Data Output** This pin is used as P-Port Data output signal for D!T-51 ICE debugger.

3.8. Power Signals

Signal Name	Pin No	I/O	Description
DVDD_18	**23, 57, 75, 107**	**P**	**Digital Core VDD** Digital core power 1.8V

DVDD_33	**9, 25, 38, 55, 73, 89, 109, 125**	**P**	**Digital I/O VDD** Digital I/O power 3.3V
DVSS	**10, 24, 39, 56, 74, 88, 108, 124**	**G**	**Digital Ground** Digital ground
PLLVDD_18	**103**	**P**	**PLL VDD** Analog PLL Power 1.8V
PLLVSS	**102**	**G**	**PLL Ground** Analog PLL Ground

4. Pin Configuration



5. Block Diagram

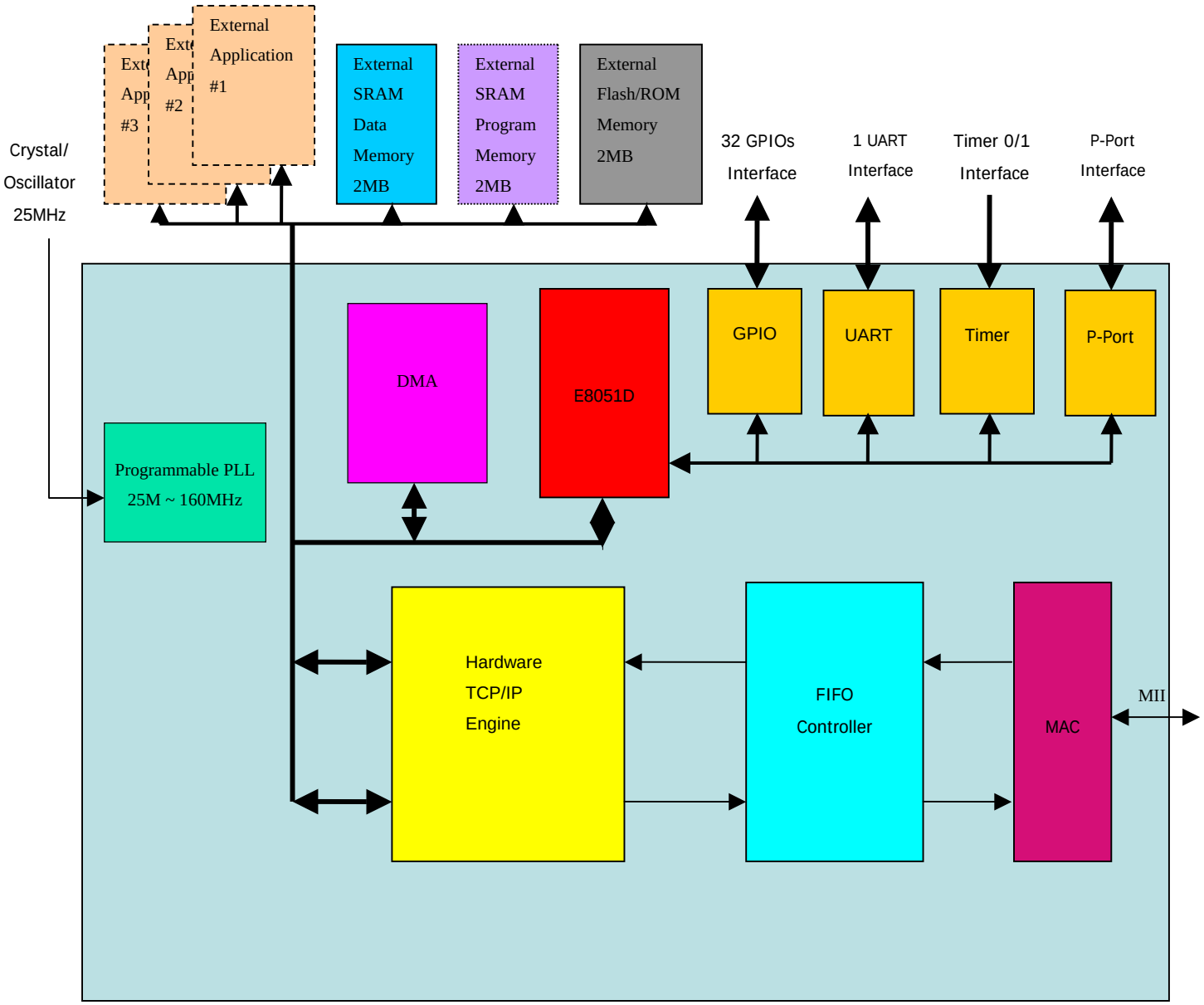


Figure 1. Block Diagram of FS8610

6. Functional Description

6.1. E8051D

E8051D is an ultra high performance 8-bit embedded controller. It has Pipelined RISC architecture 10 times faster compared to standard 8051. E8051D's 100% software compatibility with standard 8051 8-bit microcontroller is supported for software programming easily.

6.2. System Clock

FS8610 has built-in one PLL to generate system clock. The clock source of PLL is fixed to 25 MHz from crystal or oscillator. The system clock generated from PLL is programmable in the range from 25 MHz to 160 MHz. The system clock can be dynamically configured according to system requirement even the system is still running.

6.3. System Memory

FS8610 supports external Program memory and external Data memory only. It does not built-in any internal Program memory and internal Data memory. FS8610 implemets special features, Code Bank Switching, Data Memory Extension, Program Shadow RAM, On-Line Firmware Update and DMA function to enhance whole system performance.

6.3.1. Code Bank Switching Mechanism

FS8610 has implemented hardware-based Code Bank switching mechanism, so it can supports Program memory up to 2MB, which is equivalent to 32 code banks. Each code bank is 64KB in size. FS8610's program memory is no longer limited to 64KB only.

6.3.2. Data Memory Extension

FS8610 can support Data memory up to 12 MB. Data memory includes Main Data memory part and Expansion Data memory part. Main Data memory is up to 2MB maximumly. Pin DATA_CSB0 is used as chip select signal. Data memory can be extended up to 12MB by Expansion Data memory. Three external chip select signals (EXT_CSB1 ~ EXT_CSB3) can be used and programmable at specific address space.

6.3.3. Program Shadow RAM

In order to enhance the program code's running performance, FS8610 support Program Shadow RAM to run program codes at Program SRAM memory instead of at Program Flash memory. While Program Shadow RAM mode is enabled, program codes are copied from Flash memory to SRAM memory after power-on reset and executed with fast SRAM memory read/write access. While Program Shadow RAM mode is disabled, FS8610 directly runs program codes at Flash memory with lower Flash memory read/write access.

6.3.4. On-Line Firmware Update

FS8610 supports On-Line Firmware Update function to update new firmware to Flash memory and re-initializes system from remote station. On-Line Firmware Update function can only be activated at Program Shadow RAM enable mode.

6.3.5. DMA

FS8610 supports DMA function to copy one bulk data from block to another on the external Data memory. The size of each data transfer can be 0 bye to 64K bytes maximumly. While byte length is set to 0 byte, DMA function is not activated. While DMA function is activated, MCU-E8051D is idle until DMA is complete.

6.4. MII Interface

FS8610 supports 10BASE-T and 100BASE-TX compliant with 802.3 and IEEE 802.3u. Full duplex mode and half duplex mode are provided at speed 10Mbps or 100Mbps. FS8610 can transmit and receive both of Ethernet packets and IEEE 802.3 packets.

FS8610 supports MAC Sync/Async flow control mechanism, which is compilant with IEEE 802.3x, to transmit and receive MAC Pause frames in order to achieve the better network transfer performance. MAC Pause frames will be automatically discarded by FS8610.

FS8610 will always monitor the PHY's link, duplex, speed status and pause capabilities through MII management interface to update the PHY's status.

6.5. VLAN

FS8610 supports transmission and receiption of untagged frame, priority-tagged frame and VLAN-tagged frame. Untagged frame doesn't include 802.1Q tag filed in the Ethernet/IEEE802.3 packet. Priority-tagged and VLAN-tagged frame includes 802.1Q tag field in the Ethernet/IEEE802.3 packet.

FS8610 supports programmable user priority level from 0 to 7, and VID (VLAN Identification) value from 1 to 4094 at tagged frame. Only one VID is supported. FS8610 can receive the tagged frame with VID value matched and CFI bit setting to 0 or 1. But it can only transmit the tagged frame with CFI bit setting to 0.

6.6. Hardware TCP/IP Engine

FS8610 supports Hardware TCP/IP Protocol Engine to greatly offload the MCU loading and to enhance the system performance. TCP/IP protocol suites like ARP, RARP, IPv4, ICMP, IGMPv2, TCP and UDP are all implemented at Hardware TCP/IP Protocol Engine. FS8610 supports four independent hardware TCP/UDP socket channels for high bandwidth TCP/UDP data transfer requirement. In the Hardware TCP/IP channels, MAC header, Q-TAG header, IP header, TCP/UDP header are all inserted and removed automatically by FS8610. Another software channel is provided to process the ICMP/IGMPv3/TCP/UDP

packets without TCP/UDP channel counts limitation. In the software channel, only MAC header, Q-TAG header and IP header is inserted and removed by FS8610. ICMP/IGMP/TCP/UDP headers are parsed by driver.

6.6.1. ARP (Address Resolution Protocol)

FS8610 supports ARP to convert 32-bit IP address to 48-bit Ethernet MAC address for Ethernet/802.3 packet. An ARP cache table of 64 entries is built-in to prevent ARP packet flooding. FS8610 provides programmable entry lifetime timer and unicast polling counter for valid entry in the ARP cache table. FS8610 will automatically reply from other host's ARP request packet. While no ARP reply packet is received for specific ARP request from FS8610, an ARP host non-exist interrupt is asserted to specify the host is non-exist. In order to detect IP address confliction, FS8610 will broadcast Gratuitous ARP packets or check the received ARP Request packets from others.

The ARP features that FS8610 implemts are listed below.

- Support ARP Request and Reply
- Support ARP Cache Table for 64-Entries
- Support ARP Entry validation
  - Support Entry timeout
  - Support Entry unicast-poll
- Support sending Gratuitous ARP for IP conflict detection
- Support automatic detecting IP conflict from incoming ARP Request

6.6.2. RARP (Reverse Address Resolution Protocol)

FS8610 supports RARP to get the assigned 32-bit IP address from RARP server. While RARP function is enabled, FS8610 will start to transmit broadcast RARP Request packets continuously until the RARP Reply packet is received from RARP server or the RARP timer is timeout. Then RARP module will generate a RARP IP Address Assignment interrupt or a RARP Timeout interrupt to notify system driver.

The RARP features that FS8610 implemts are listed below.

- Support RARP Request
- Support RARP retransmission and timeout

6.6.3. IP (Internet Protocol)

FS8610 supports IP version 4 only. Any IP packet is not version 4 will be silently discarded. FS8610 will automatically generate and remove IP header including IP options field and padding field. Any packet with IP header checksum error is discarded silently.

FS8610 only supports IP address Class A, B, C and D. IP address Class E packet is not supported and will be silently discarded. FS8610 supports Unicast, Muticast and Broadcast IP packets transmission and receipt. 4 sets of IP Group Address are programmable and can be transmited or received by FS8610 to join or leave Muticast Group. FS8610 can receive the multicast IP packet which belongs to the joined muticast Groups. FS8610 supports three types of IP broadcast packets: Limited Broadcast packet (255.255.255.255), Network (Class A/B/C) Broadcast packet and Subnet (Class A/B/C) Broadcast pacekt. Limited Broadcast IP packet will be limited on the local network. It will be blocked by router and can't be forwarded to other network. Network Broadcast IP packet and Subnet Broadcast IP packet will be forwarded to other network by router.

FS8610 supports IP packet fragmentation. The IP payload can be up to 64KB in length. FS8610 does not support IP packets reassembly. All of the received fragmented IP packets are reassembled by driver.

The IP features that FS8610 implemts are listed below.

- Support IPv4 protocol only (IPv6 packet will be silently discarded)
- Support IP header checksum generation and verification
- Support IP limited broadcast, directed network broadcast, directed subnet broadcast, directed all-subnet broadcast
- Support four sets of IP group address
- Support IP Fragmentation
- Support Identification (ID) field programmable
- Support Type-of-Service (TOS) field programmable
- Support Time-to-Live (TTL) field programmable
- Support IP header checksum generation and validation

6.6.4. ICMP (Internet Control Message Protocol)

FS8610 supports to transmit and receive ICMP packets. ICMP header is generated and removed by FS8610. Any packet with ICMP header checksum error is discarded silently. The Type and Code fields of ICMP header is parsed by driver.

The ICMP features that FS8610 implemts are listed below.

- Support all ICMP error message
- Support all ICMP query message
- Support ICMP header checksum field generation and validation
- Support transmitting fragmented ICMP message

6.6.5. IGMP (Internet Group Management Protocol)

IGMP is used to report IP multicast group membership to neighboring multicast routers. FS8610 only supports both of IGMP version 1 & version 2 packet without driver‘s interpretation. IGMP version 3 packet will be received, transmitted and parsed by driver. Any packet with IGMP header checksum error is silently discarded. FS8610 supports 4 sets of IP group address for IP multicasting usage. Join or leave the specified group is controlled by driver.

The IGMP features that FS8610 implemts are listed below.

- Support IGMPv2 and compliant with IGMPv1
- Support 4 Group Address join and leave
- Support Router Alert IP option
- Support IGMP header checksum field generation and validation

6.6.6. UDP (User Datagram Protocol)

FS8610 supports to transmit and receive UDP packets. UDP header is generated and removed by FS8610. Any packet with UDP header checksum error is discarded silently.

While transmitting a UDP packet, driver only needs to write UDP payload into UDP socket channel FIFO. FS8610 will automatically insert MAC/IP/UDP header before UDP payload and append CRC filed to assembly one Ethernet/802.3 packet for transmitting.

While receiving a UDP packet, FS8610 will remove MAC/IP/UDP header and write UDP payload filed into socket channel FIFO. UDP channel can be programmed to accept UDP packet destinated to local port number with Single Unicast IP address, All Unicast IP address, Multicast IP address and Broadcast IP address.

The UDP features that FS8610 implemts are listed below.

- Support client/server mode
- Support to transmit single unicast, all unicast, multicast or broadcast packets
- Support to receive single unicast, all unicast, multicast or broadcast packets
- Support UDP header checksum generation and validation
- Support not to generate checksum (transmit all 0’s checksum field)
- Support not to validate checksum (receive all 0’s checksum field)
- Support transmitting fragmented UDP datagram

6.6.7. TCP (Transmission Control Protocol)

FS8610 supports to transmit and receive TCP packets. TCP header is generated and removed by FS8610. Any packet with TCP header checksum error is discarded silently.

FS8610 can easily establish TCP channel connection and termination by driver's register setting. After each TCP channel is connected well, driver can read and write TCP payload directly through socket channel interface directly. While transmitting TCP packets, FS8610 automatically reads TCP payload from socket FIFO, inserts MAC/IP/TCP header before TCP payload and appends CRC filed to assembly one Ethernet/802.3 packet. While receiving TCP packets, FS8610 automatically removes MAC/IP/TCP header and writes TCP payload into socket FIFO.

The TCP features that FS8610 implemts are listed below.

- Support client/server mode
- Support Push flag transmit and receive
- Support Urgent pointer to transmit and receive Urgent data
- Support programmable MSS (Maximum Segment Size)
- Support TCP header checksum generation and validation
- Support programmable initial sequence number
- Support simultaneous Open state
- Support receiving RST segment
- Support programmable delayed ACK
- Support Sliding Window for bulk data transfer
- Support programmable Persist Timer for probing zero window
- Support Silly Window Syndrome (SWS) Avoidance algorithm
- Support programmable Fast Retransmission for out-of-order TCP segments
- Support programmable Retransmission Timeout (RTO) with exponential backoff
- Support MSS option at TCP option field

6.7. PPPoE (Point-to-Point Protocol over Ethernet)

FS8610 supports PPPoE to connect remote hosts over xDSL device. FS8610 can transmit and receive all PPPoE control packets at Discoverage stage and Session satge. Once PPPoE session is established and IP address is assigned, FS8610 can transmit and receive PPPoE IP (data) packets.

FS8610 supports retransmition and timout for PADI/PADR//LCP configure request/LCP terminate request/NCP configure request /PAP request packets. PPP (Point-to-Point Protocol) are implemented by driver. It includes LCP (Link Control Protocol), PAP (Password Authentication Protocol) and IPCP (Internet Protocol Control Protocol).

6.8. UART

FS8610 supports one high speed UART interface for serila port connection. The UART port can be programmed into Synchronous or Asynchronous mode, Fixed rate or flexible rate. The UART features are listed as below.

- Baud Rate: 1200 ~ 230400
- Data Bits: 7 or 8
- Parity Bit: Even, Odd or None
- Stop Bit: 1
- Flow Control: Hardware (RTS/CTS), Software (Xon/Xoff), None

6.9. GPIO

FS8610 supports 32 GPIOs interface for general purpose application. With the E8051D's high system performance, versatile interfaces like I^2C master, I^2C slave, I^2S and SPI can be emulated easily through GPIO interface by driver.

6.10. SRAM-based External Expansion Interface

FS8610 supports SRAM-based External Expansion interface for external SRAM extensions (above 2MB) or E8051D controllabe devices like JPEG Encoder for IP-CAM application. At most, three external chip select signals (EXT_CSB1 ~ EXT_CSB3) can be activated and programmed at specific address space.

6.11. System Standby & Wake-On-LAN (WOL)

FS8610 supports Standby mode and Shut Down mode to save power consumption. While system is forced into Standby mode, FS8610 can be resumed from wake-up events. Wake-up events includes Magic packet, PHY's Link Status Change and External interrupt. While system is forced into Shut Down mode, FS8610 can only be restarted from Power-on Reset. Shut Down mode is more power saving than Standby mode.

6.12. P-Port ICE Debug Interface

FS8610 supports P-Port ICE Debug interface for software development. With FASP-8610 Development Board and D!T-51 Debug Tool which are provided by FameG, software developmet is easy and efficient for user.

7. System Diagram

7.1. Program Shadow RAM Enable (Single Code Bank)

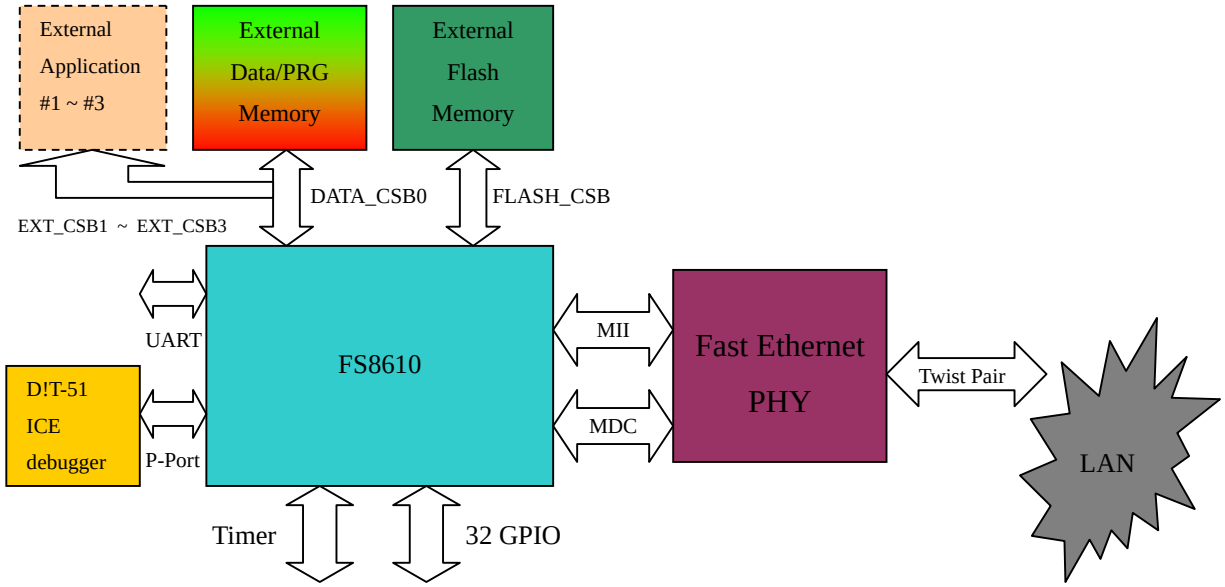


Figure 2. System Diagram of FS8610 with Program Shadow RAM Enable (Single Code Bank)

7.2. Program Shadow RAM Enable (Multiple Code Banks)

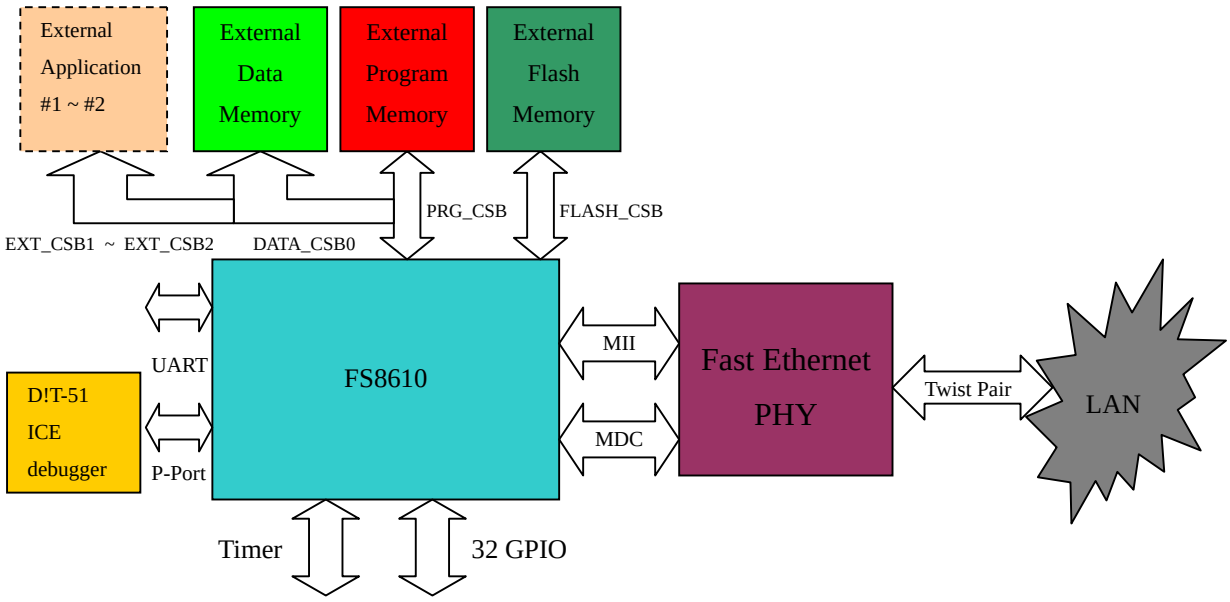


Figure 3. System Diagram of FS8610 with Program Shadow RAM Enable (Multiple Code Banks)

7.3. Program Shadow RAM Disable

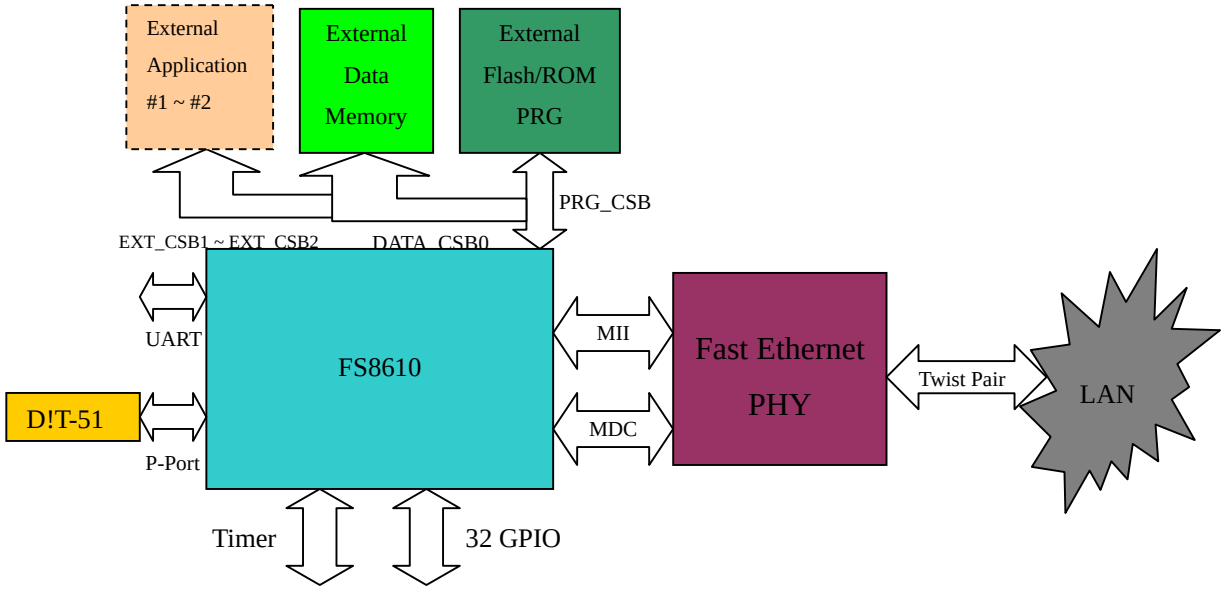


Figure 4. System Diagram of FS8610 with Shadow RAM Disable

8. Electrical Characteristics

8.1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DDC}	Core Supply Voltage (DVDD_18)	-0.5	2.5	V
V_{DDPLL}	PLL Supply Voltage (PLLVDD_18)	-0.5	2.5	V
V_{DDIO}	I/O Supply Voltage (DVDD_33)	-0.5	4.6	V
V_{IN}	Input Voltage	-0.5	6	V
V_{OUT}	Output Voltage	-0.5	4.6	V
T_A	Operating Temperature	0	70	℃
T_S	Storage Temperature	-65	150	℃

8.2. Power Consumption (DVDD_33 = 3.3V, DVDD_18 = PLLVDD_18 = 1.8V, TA = 25℃)

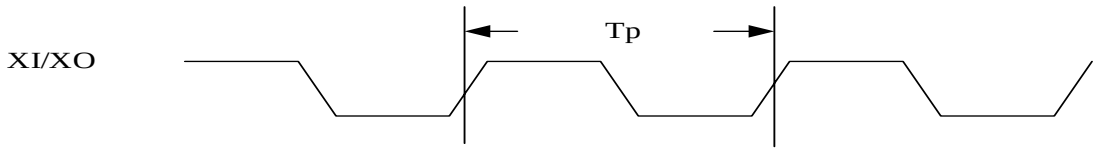
Symbol	Parameter	Condition	Max		Unit
IDD_{NOR}	Normal mode current	@ 25MHz system clock, Full channels	@3.3V	15	mA
			@1.8V	45	mA
		@ 100MHz system clock, Full channels	@3.3V	25	mA
			@1.8V	135	mA
		@ 160MHz system clock, Full channels	@3.3V	35	mA
			@1.8V	195	mA
IDD_{STB}	Standby mode current (system resumed by wake-up event)	@ 25MHz ~ 160MHz system clock	@3.3V	100	uA
			@1.8V	20	mA
IDD_{SHD}	Shut Down mode current (system resumed by Power-on Reset)	@ 25MHz ~ 160MHz system clock	@3.3V	100	uA
			@1.8V	200	uA

8.3. DC Characteristics (DVDD_33 = 3.0V ~ 3.6V, DVDD_18 = PLLVDD_18 = 1.62V ~ 1.98V, TA = 25℃)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
DVDD_18	Core Supply Voltage		1.62	1.8	1.98	V
PLLVDD_18	PLL Supply Voltage		1.62	1.8	1.98	V
DVDD_33	I/O Supply Voltage		3.0	3.3	3.6	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2.0		5.5	V
V_{OL}	Output Low Voltage	I_{OL}=4.0mA			0.4	V
V_{OH}	Output High Voltage	Ioh=-4.0mA	2.4			V
I_{IL}	Input Leakage Current				+/- 10	uA
I_{OL}	Tristate Output Leakage Current				+/- 10	uA

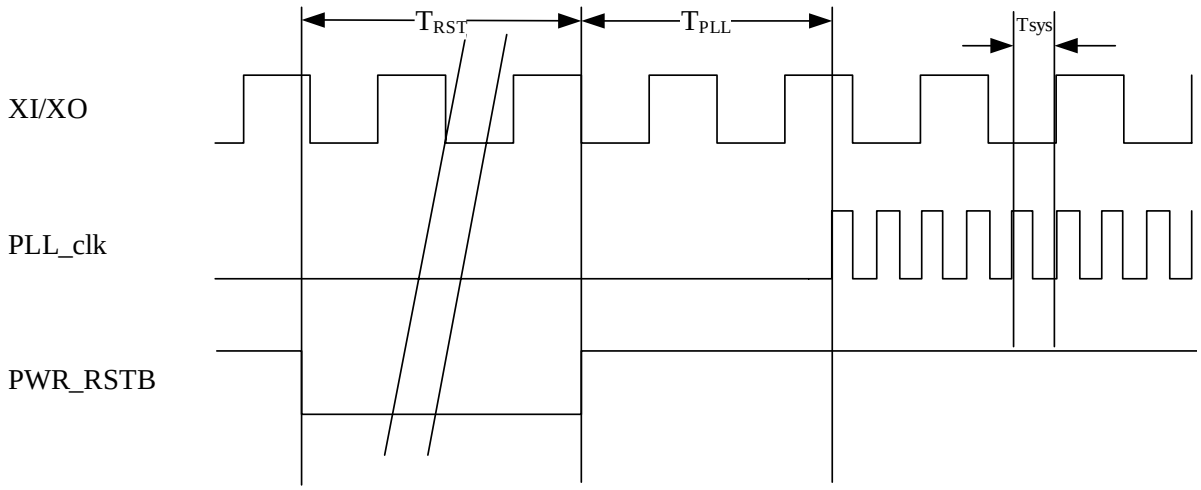
8.4. AC Characteristics (DVDD_33 = 3.0V ~ 3.6V, DVDD_18 = PLLVDD_18 = 1.62V ~ 1.98V, TA = 25℃)

8.4.1. Crystal/Oscillator Timing



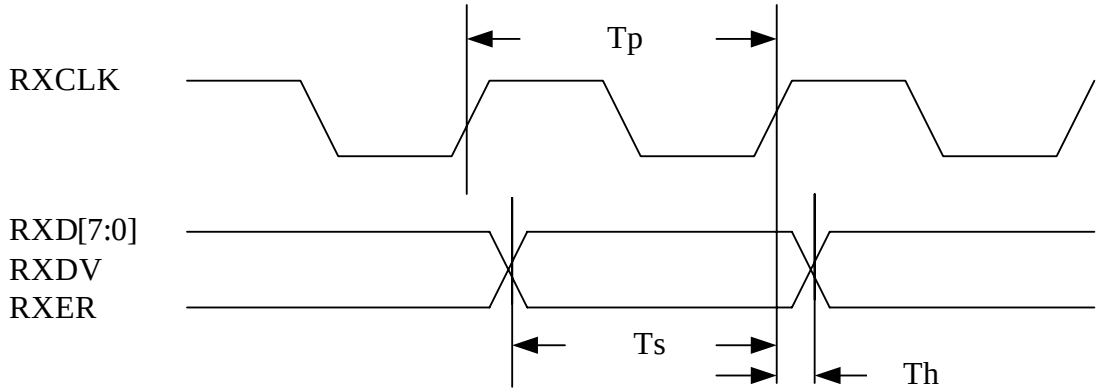
Symbol	Description	Min	Typ	Max	Unit
Tp	Period of XI/XO	40	40	40	ns

8.4.2. Power-on Hardware Reset and PLL Clock Timing



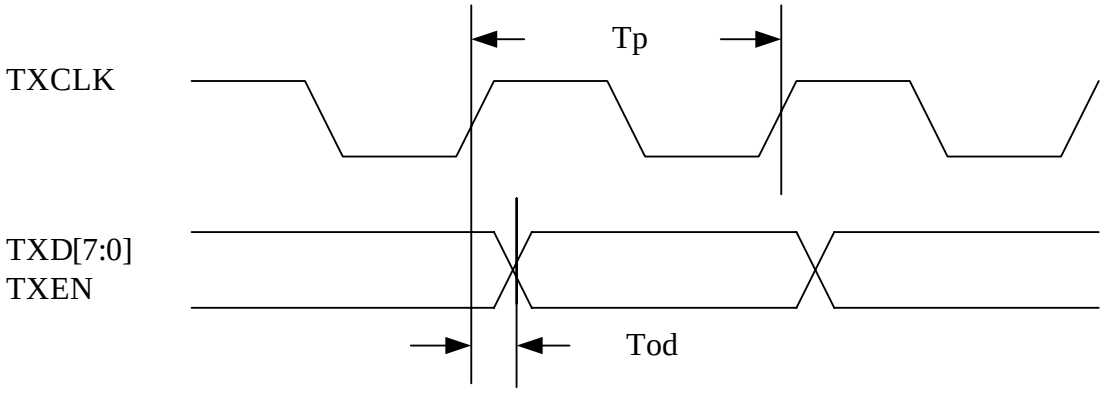
Symbol	Description	Min	Typ	Max	Unit
T_{RST}	Power-on Hardware Reset	100			ms
T_{PLL}	PLL lock duration	50			us
T_{sys}	System Clock period	6.3		40	ns

8.4.3. MII Receiving Timing



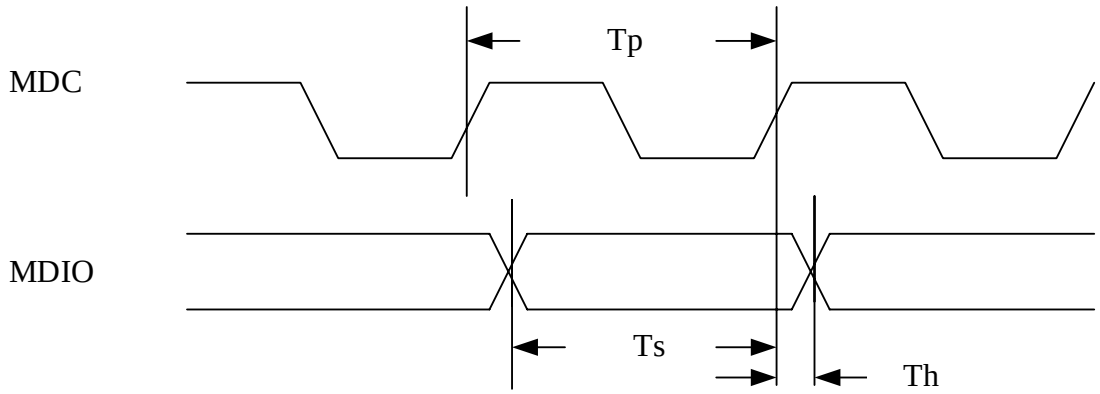
Symbol	Description	Min	Typ	Max	Unit
Tp	Period of RXCLK 100M 10M		 40 400		 ns
Ts	Setup time of RXD[7:0], RXDV, RXER	2			ns
Th	Hold time of RXD[7:0], RXDV, RXER	2			ns

8.4.4. MII Transmitting Timing



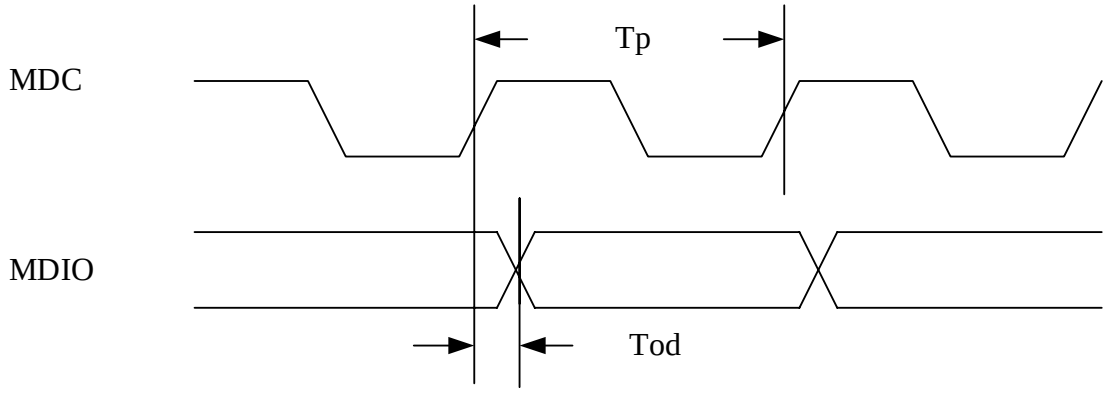
Symbol	Description	Min	Typ	Max	Unit
Tp	Period of TXCLK 100M 10M		 40 400		 ns
Tod	Output Delay of TXD[7:0], TXEN, TXER			8	ns

8.4.5. MII Management Read Timing



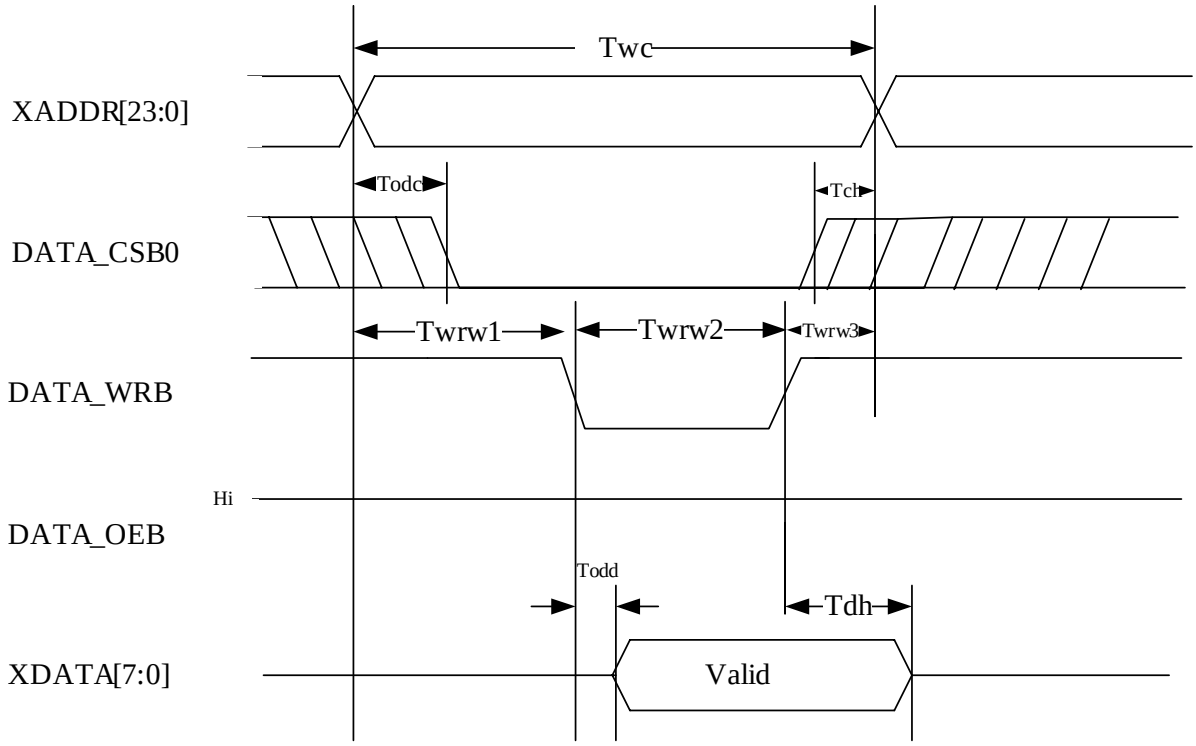
Symbol	Description	Min	Typ	Max	Unit
Tp	Period of MDC	400		787	ns
Ts	Setup time of MDIO	6			ns
Th	Hold time of MDIO	0			ns

8.4.6. MII Management Write Timing



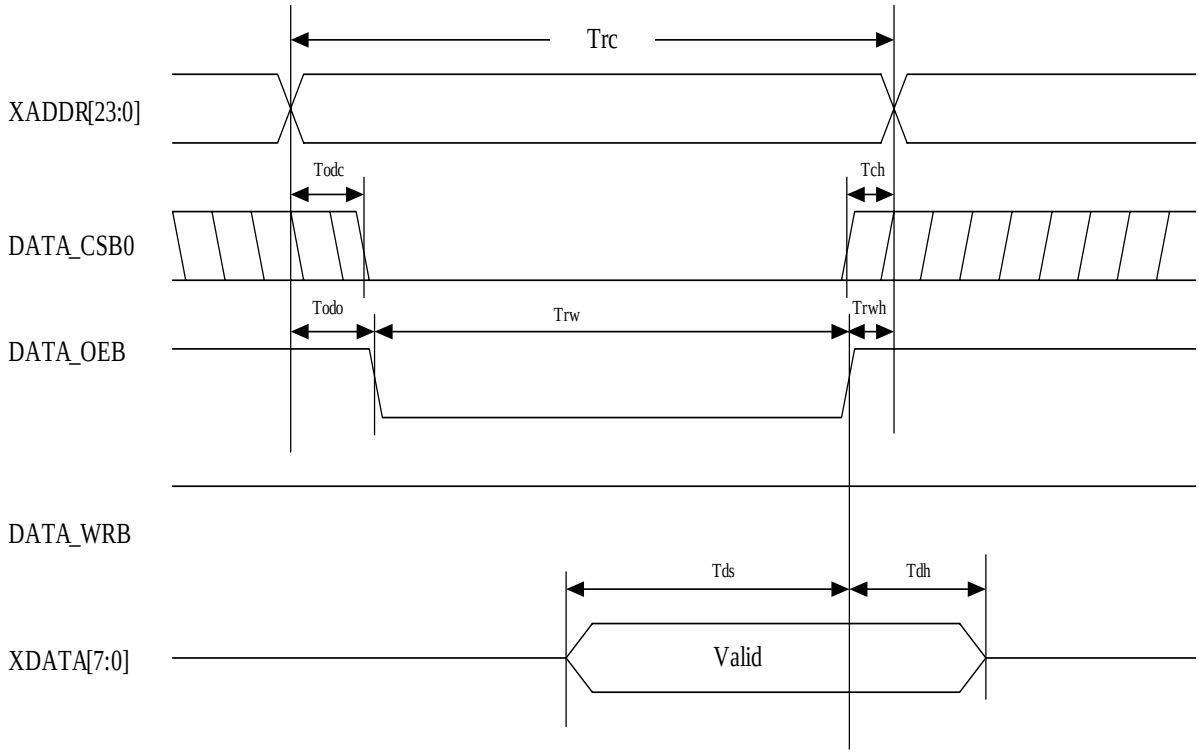
Symbol	Description	Min	Typ	Max	Unit
Tp	Period of MDC	400		787	ns
Tod	Output Delay of MDIO Tp = 400ns Tp = 787ns			 211 410	 ns

8.4.7. External Main Data Memory Bus Write Timing



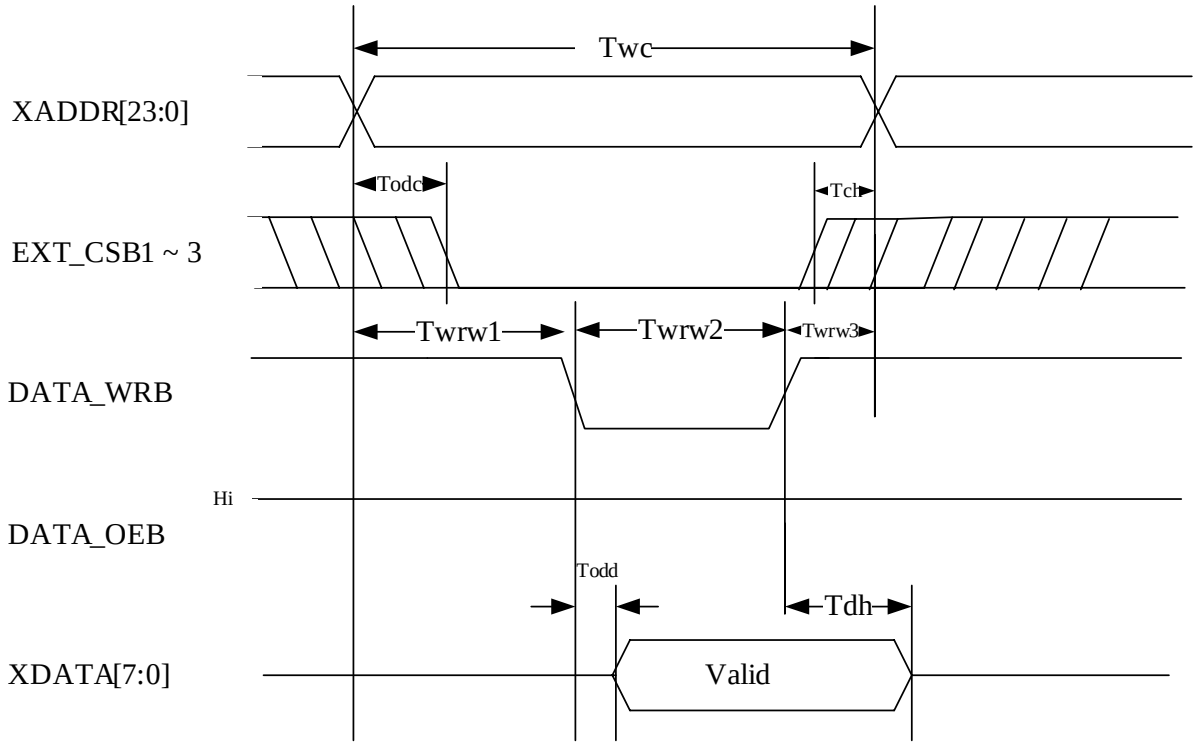
Symbol	Description	Min	Typ	Max	Unit
Twc	Write Cycle Time of XADDR	3 * T_{sys}		18 * T_{sys}	ns
Todc	Output Delay of DATA_CSB0		1 * T_{sys}		ns
Tch	Hold Time of DATA_CSB0		1 * T_{sys}		ns
Twrw1	Write Width 1 of DATA_WRB		1 * T_{sys}		ns
Twrw2	Write Width 2 of DATA_WRB	1 * T_{sys}		16 * T_{sys}	ns
Twrw3	Write Width 3 of DATA_WRB		1 * T_{sys}		ns
Todd	Output Delay Time of XDATA			0	ns
Tdh	Data Hold Time of XDATA		1 * T_{sys}		ns

8.4.8. External Main Data Memory Bus Read Timing



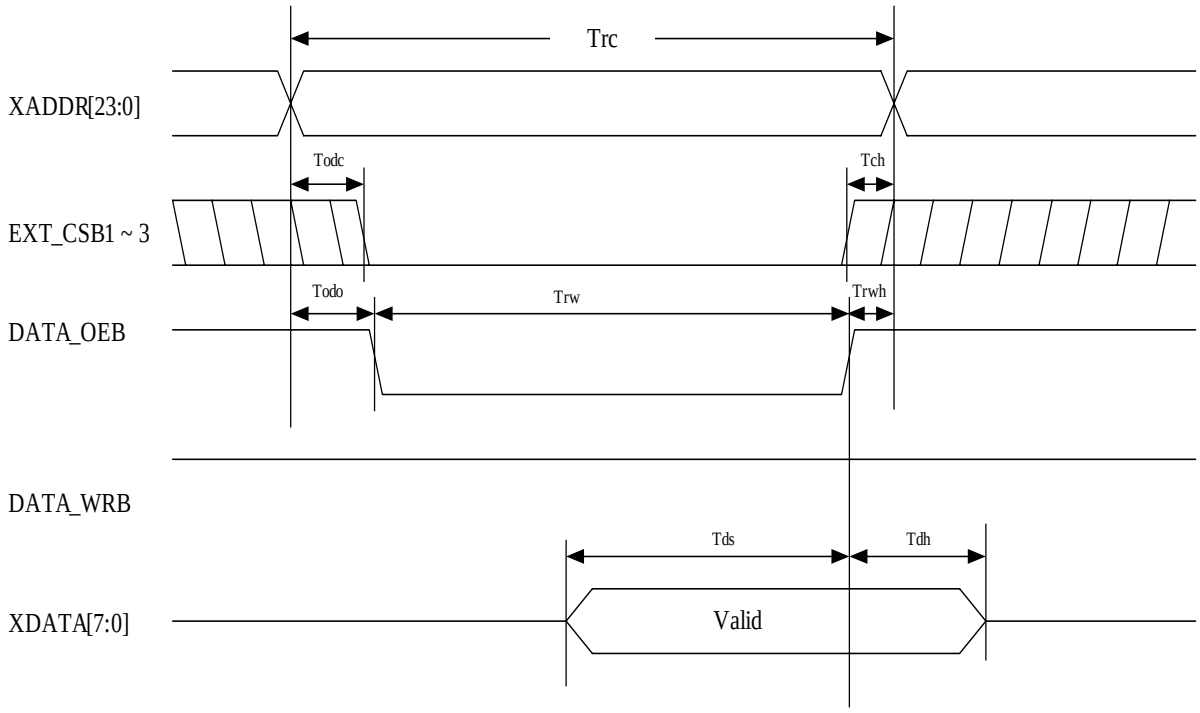
Symbol	Description	Min	Typ	Max	Unit
Trc	Read Cycle Time of XADDR	$2 * T_{sys}$		$17 * T_{sys}$	ns
Todc	Output Delay of DATA_CSB0			0	ns
Tch	Hold Time of DATA_CSB0			0	ns
Todo	Output Delay of DATA_OEB0			0	ns
Trw	Read Width of DATA_OEB	$2 * T_{sys}$		$17 * T_{sys}$	ns
Trwh	Read Hold Time of DATA_OEB			0	ns
Tds	Data setup Time of XDATA	8.5			ns
Tdh	Data Hold Time of XDATA	0.5			ns

8.4.9. External Application Expansion Bus Write Timing



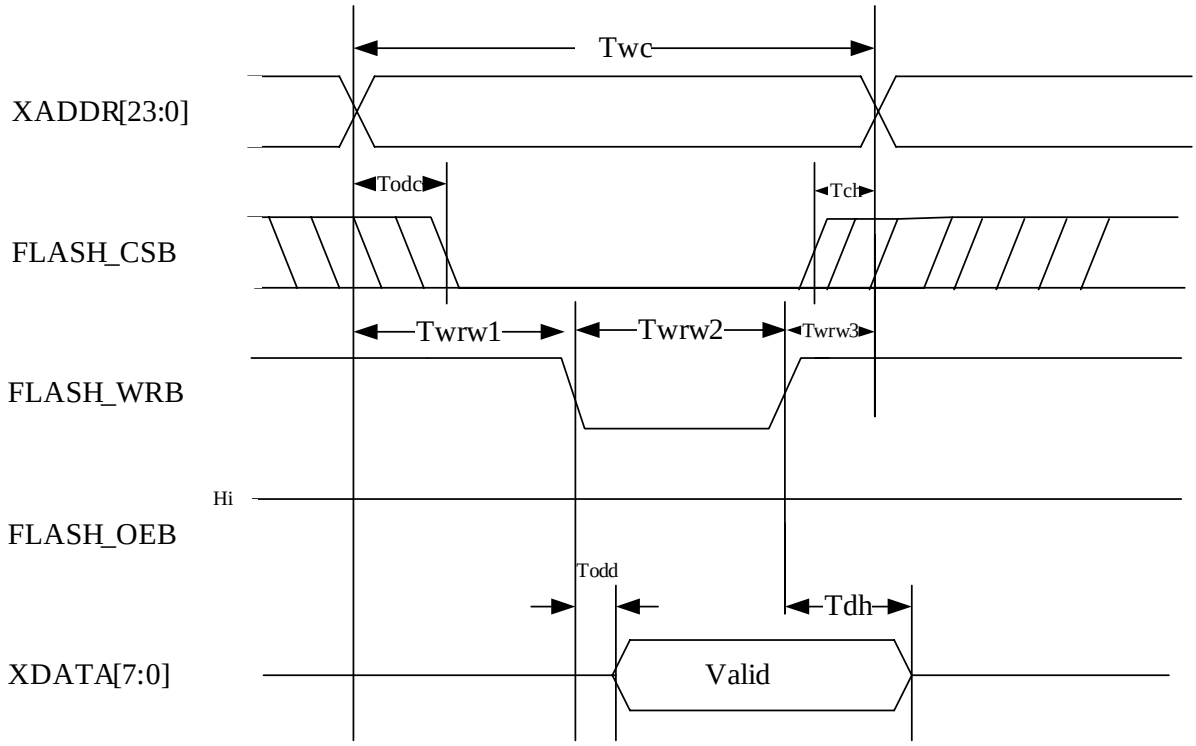
Symbol	Description	Min	Typ	Max	Unit
Twc	Write Cycle Time of XADDR	4 * T_{sys}		18 * T_{sys}	ns
Todc	Output Delay of EXT_CSB1 ~ 3			0	ns
Tch	Hold Time of EXT_CSB1 ~ 3			0	ns
Twrw1	Write Width 1 of DATA_WRB		1 * T_{sys}		ns
Twrw2	Write Width 2 of DATA_WRB	1 * T_{sys}		15 * T_{sys}	ns
Twrw3	Write Width 3 of DATA_WRB		2 * T_{sys}		ns
Todd	Output Delay Time of XDATA			0	ns
Tdh	Data Hold Time of XDATA		2 * T_{sys}		ns

8.4.10. External Application Expansion Bus Read Timing



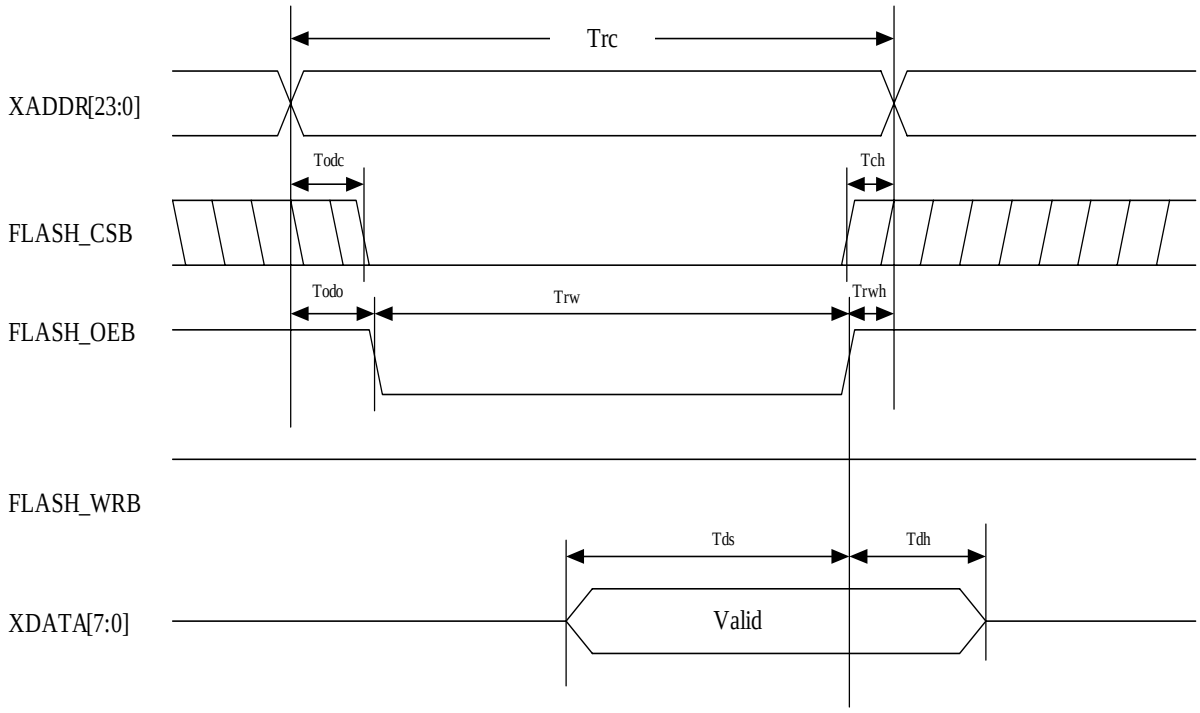
Symbol	Description	Min	Typ	Max	Unit
Trc	Read Cycle Time of XADDR	$2 * T_{sys}$		$16 * T_{sys}$	ns
Todc	Output Delay of EXT_CSB1 ~ 3			0	ns
Tch	Hold Time of EXT_CSB1 ~ 3			0	ns
Todo	Output Delay of DATA_OEB0			0	ns
Trw	Read Width of DATA_OEB	$2 * T_{sys}$		$16 * T_{sys}$	ns
Trwh	Read Hold Time of DATA_OEB			0	ns
Tds	Data setup Time of XDATA	8.5			ns
Tdh	Data Hold Time of XDATA	0.5			ns

8.4.11. External Flash/ROM Memory Bus Write Timing



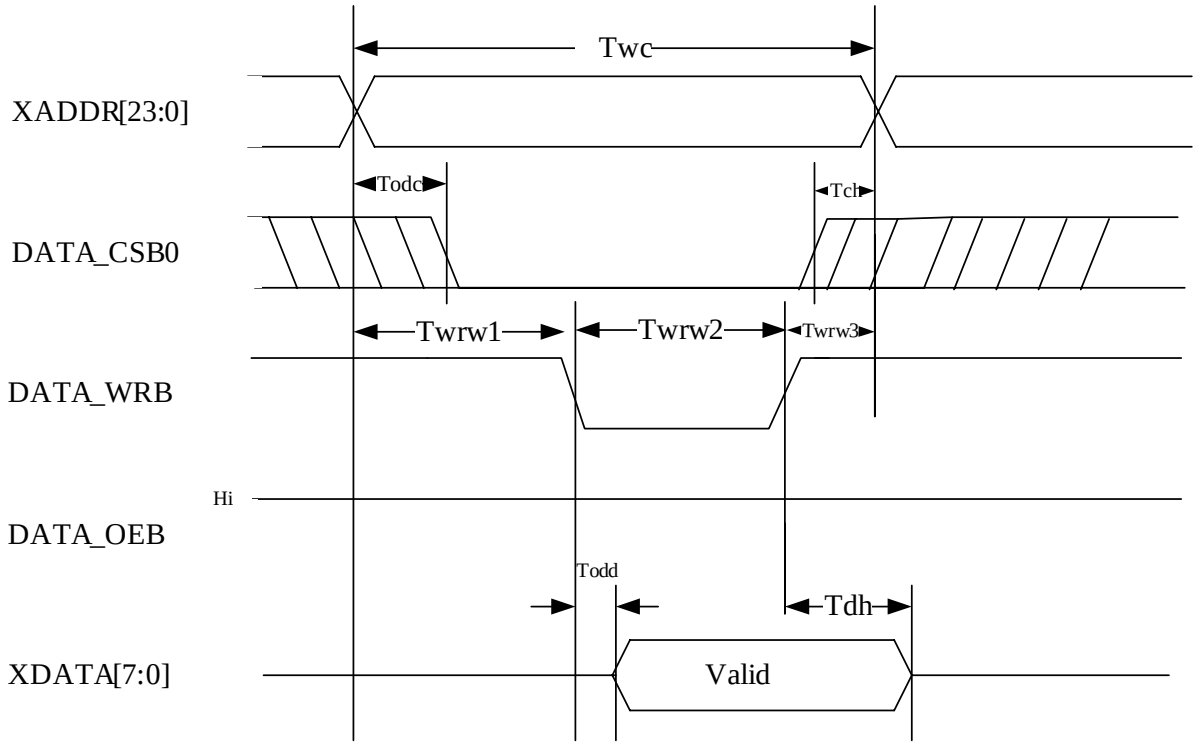
Symbol	Description	Min	Typ	Max	Unit
Twc	Write Cycle Time of XADDR	11 * T_{sys}		18 * T_{sys}	ns
Todc	Output Delay of FLASH_CSB			0	ns
Tch	Hold Time of FLASH_CSB			0	ns
Twrw1	Write Width 1 of FLASH_WRB		1 * T_{sys}		ns
Twrw2	Write Width 2 of FLASH_WRB	9 * T_{sys}		16 * T_{sys}	ns
Twrw3	Write Width 3 of FLASH_WRB		1 * T_{sys}		ns
Todd	Output Delay Time of XDATA			0	ns
Tdh	Data Hold Time of XDATA		1 * T_{sys}		ns

8.4.12. External Flash/ROM Memory Bus Read Timing



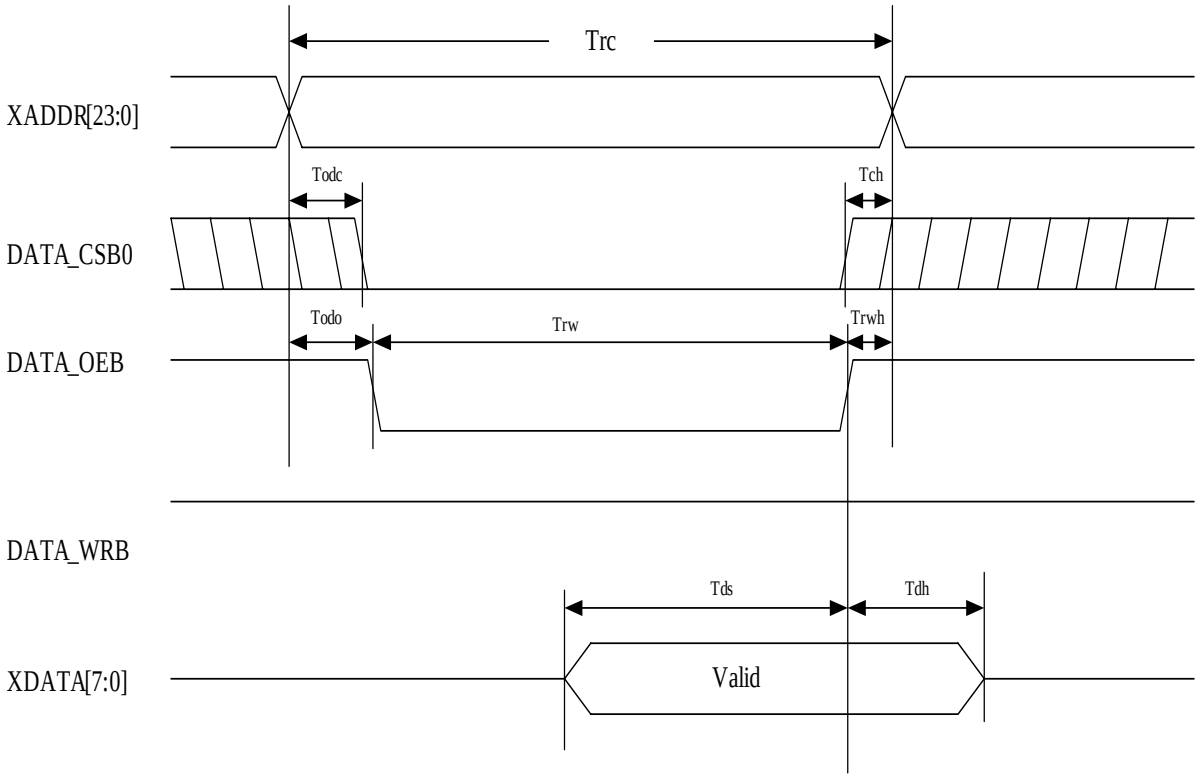
Symbol	Description	Min	Typ	Max	Unit
Trc	Read Cycle Time of XADDR	9 * T_{sys}		16 * T_{sys}	ns
Todc	Output Delay of FLASH_CSB			0	ns
Tch	Hold Time of FLASH_CSB			0	ns
Todo	Output Delay of FLASH_OEB			0	ns
Trw	Read Width of FLASH_OEB	9 * T_{sys}		16 * T_{sys}	ns
Trwh	Read Hold Time of FLASH_OEB			1.1	ns
Tds	Data setup Time of XDATA	8			ns
Tdh	Data Hold Time of XDATA	0.5			ns

8.4.13. External Program Memory Bus Write Timing



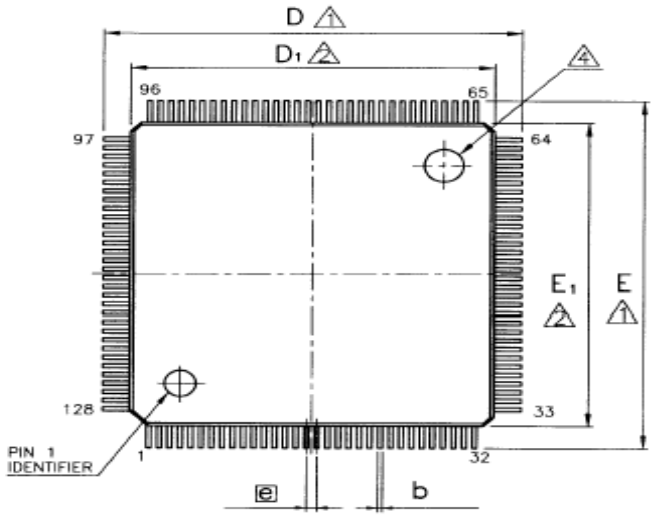
Symbol	Description	Min	Typ	Max	Unit
Twc	Write Cycle Time of XADDR	4 * T_{sys}		18 * T_{sys}	ns
Todc	Output Delay of DATA_CSB0			0	ns
Tch	Hold Time of DATA_CSB0			1 * T_{sys}	ns
Twrw1	Write Width 1 of DATA_WRB		1 * T_{sys}		ns
Twrw2	Write Width 2 of DATA_WRB	9 * T_{sys}		16 * T_{sys}	ns
Twrw3	Write Width 3 of DATA_WRB		1 * T_{sys}		ns
Todd	Output Delay Time of XDATA			0	ns
Tdh	Data Hold Time of XDATA		1 * T_{sys}		ns

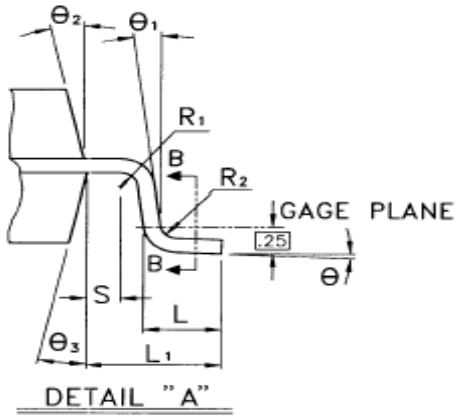
8.4.14. External Program Memory Bus Read Timing

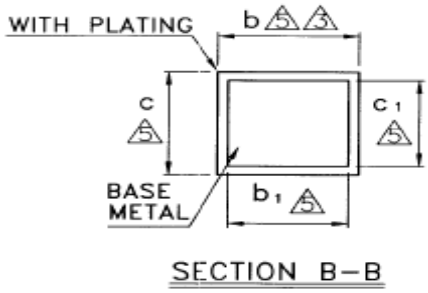


Symbol	Description	Min	Typ	Max	Unit
Trc	Read Cycle Time of XADDR	$2 * T_{sys}$		$8 * T_{sys}$	ns
Todc	Output Delay of DATA_CSB0			0	ns
Tch	Hold Time of DATA_CSB0			0	ns
Todo	Output Delay of DATA_OEB			0	ns
Trw	Read Width of DATA_OEB	$2 * T_{sys}$		$8 * T_{sys}$	ns
Trwh	Read Hold Time of DATA_OEB			0	ns
Tds	Data setup Time of XDATA	8.5			ns
Tdh	Data Hold Time of XDATA	0.5			ns

9. 128L LQFP Package Dimension (14 x 14 x 1.4 mm)







Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	—	0.002	—	—
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		

10. Revision History

Release	Date	Author	Modification
0.1	09/04/2006	Huai-Chih Ma	1. Initial Release.
0.2	10/11/2006	Huai-Chih Ma	1. Update Shadow SRAM function description.
1.0	12/26/2006	Huai-Chih Ma	1. Update Power Consumption current value at all operation modes.
1.1	01/31/2007	Huai-Chih Ma	1. Modify the pin name of pin 103, 126 ~ 128 of Pin Configuration block to match with Pin Description name. 2. Remove DoCD character
2.0	02/14/2007	Huai-Chih Ma	1. Update Generation Descriptions, Features, Block Diagram and Functional Description.