DATA SHEET

(DOC No. HX8312-A-DS)

HX8312-A

240RGB x 320 dot, 262,144 color
TFT controller driver
with internal RAM

Preliminary version 03 November, 2005

Himax Technologies, Inc.
http://www.himax.com.tw

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General Description

This manual describes the Himax's HX8312-A 240RGB*320 dots resolution driving controller. The HX8312-A is designed to provide a single-chip solution that combined a gate driver, a source driver, power supply circuit, and internal graphics SRAM for 262,144 colors to drive a TFT panel with 240RGB*320 dots at maximum.

The HX8312-A can be operated in low-voltage (1.65V) condition to the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, the HX8312-A also supports various functions to reduce the power consumption of a LCD system via software control, such as an standby mode and 8-color display mode. The HX8312-A has five system interfaces: an I80-system and M68-system 18-/16-/9-/8-bit bus interface, VSYNC interface(internal clock, DB17-0) , serial data transfer interface and RGB18-/16-/6-bit bus interface(DOTCLK, VSYNC, HSYNC, ENABLE). In RGB interface and VSYNC interface mode, the combined use widow address function enables to display data in a moving picture area and data in internal RAM at once, which makes it possible to transfer display data only when rewriting a screen and minimize data transfers.

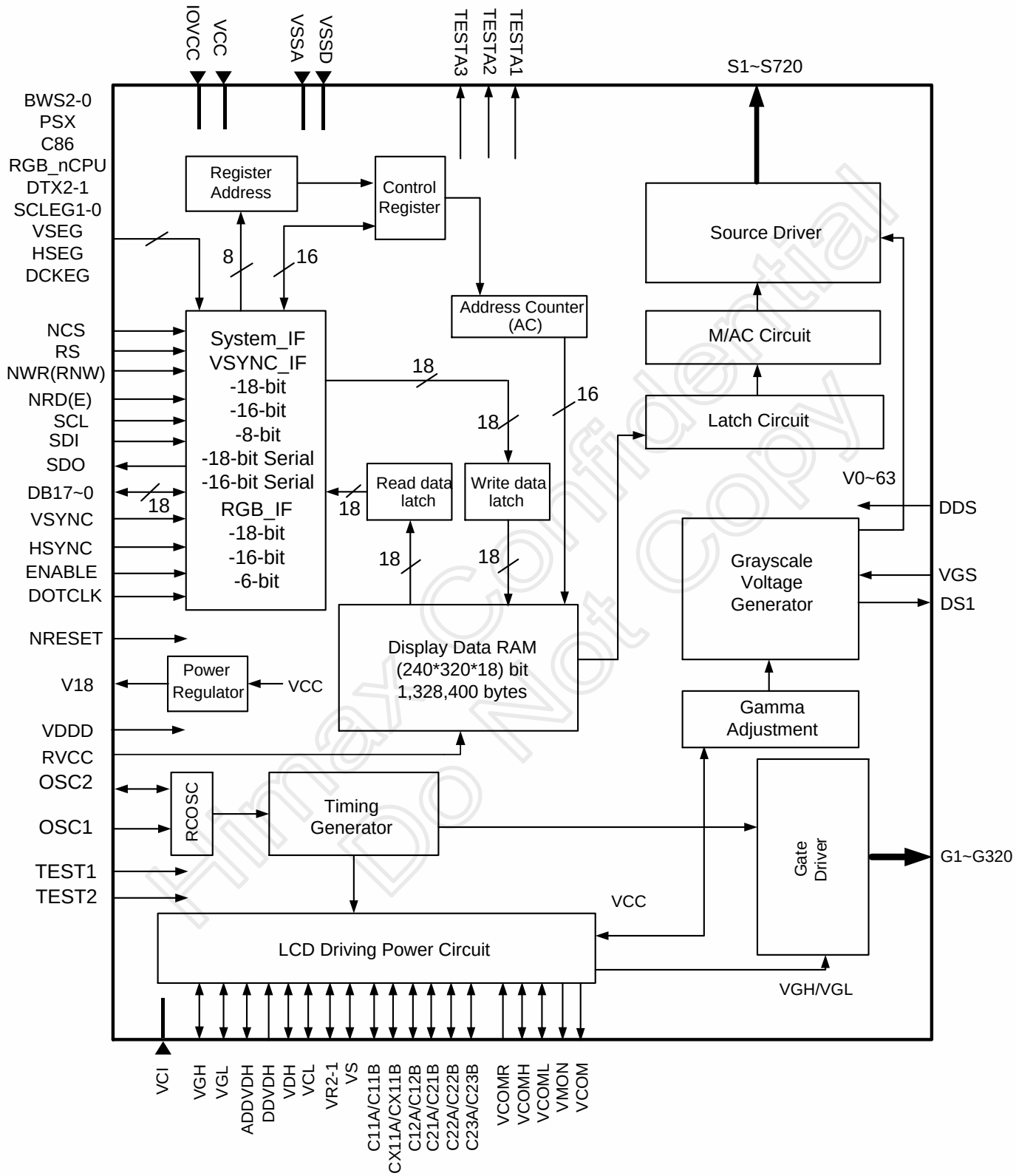
The HX8312-A is suitable for any small portable battery-driven product and requiring long-term driving capabilities, such as small PDAs, digital cellular phones and bi-directional pagers

Features

- Single chip solution to drive a TFT panel
- 240RGB x 320-dot graphics display LCD controller/driver and 262,144 TFT colors
- Support interface:
  - System interface
    (I80 / M68) parallel bus system interface
    Serial bus system interface
  - RGB interface
  - VSYNC interface
- Internal graphics RAM capacity: 1,328,400 bytes
- The 262,144 colors can be displayed at the same time with gamma correction
- The vertical scroll display function in line units
- Internal operation circuit of liquid crystal display:
  - Source channel: 720
  - Gate line: 320
- To write data in a window-RAM address area by using a window address area access function
- Low-power consumption architecture supports:
  - VCI = 2.5 to 3.3 V (internal reference voltage)
  - VCC = 2.2 to 3.3 V (corresponding low-voltage operation)
  - IOVCC = 1.65 to 3.3 V (Interface I/O operation)
  - VLCD=4.5~5.5V
  - Power-saving functions
    - 8-color mode
    - standby mode
- N-line inversion AC liquid-crystal drive
- Partial liquid crystal drive to display two screens at arbitrary positions
- Internal oscillator and hardware / software reset function

1. Device Overview

1.1 Block Diagram



1.2 Pin Description

Input Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
BWS2	I	1	MPU	The bus width selection in RGB interface circuit. 0: 18-bit, 1: 16-bit
BWS1-0		2	MPU	The bus width selection in system interface circuit. (see Table 2. 1)
PSX	I	1	MPU	The parallel and serial bus interface selection in system interface circuit. 0: Parallel bus interface, 1: Serial bus interface
NCS	I	1	MPU	Chip select signal. 0: chip can be accessed; 1: chip cannot be accessed.
NRESET	I	1	MPU	Reset pin. Setting either pin low initializes the LSI. Must be reset the chop after power being supplied.
NRD (E)	I	1	MPU	I80 system: Serves as a read signal and reads data at the low level. M68 system: 0: Read/Write disable ; 1: Read/Write enable Fix it to IOVCC or VSSD level when using serial buss interface.
NWR (RNW)	I	1	MPU	I80 system : serves as a write signal and writes data at the rising edge. M68 system: 0: Write ; 1: Read Serial bus interface: 0: Write ; 1: Read
C86	I	1	MPU	MPU selection 0: i80 series MPU; 1: M68 series MPU. Fix it to IOVCC or VSSD level when using serial bus interface.
SDI	I	1	MPU	Serial bus interface data input pin. Fix it to IOVCC or VSSD level when using parallel bus interface.
SCL	I	1	MPU	Serial bus interface clock input pin Fix it to IOVCC or VSSD level when using parallel bus interface.
RGB_nCPU	I	1	MPU	0: System interface can be accessed. 1: System interface can not be accessed.
RS	I	1	MPU	Command/display Data Selection 0: Command, 1: Display data
DTX2-1	I	2	MPU	Specify the transferring method of one pixel data in system interface. (see Table 2. 3)
SCLEG1-0	I	1	MPU	Determine the effective edge operation of SCLK for SDI data latch and SDO data output. (see Table 2. 6)
VSYNC	I	1	MPU	Vertical synchronization signal input pin. Must be connected to IOVCC if not in use.
HSYNC	I	1	MPU	Horizontal synchronization signal input pin. Must be connected to IOVCC if not in use.
DOTCLK	I	1	MPU	Dot clock signal input used in the RGB interface circuit. Must be connected to IOVCC if not in use.
ENABLE	I	1	MPU	Enable signal pin used in RGB interface circuit. 0: disable, 1: enable when EPL (D1 bit of R157) = 0. 0: enable, 1: disable when EPL (D1 bit of R157) = 1. Must be connected to IOVCC if not in use.
VSEG	I	1	MPU	Valid VSYNC polarity selection pin 0: Start in the low level, 1: Start in the high level Fix it to IOVCC or VSSD level when only using system interface.
HSEG	I	1	MPU	Valid HSYNC polarity selection pin 0: Start in the low level, 1: Start in the high level. Fix it to IOVCC or VSSD level when only using system interface.
DCKEG	I	1	MPU	Valid DOTCLK polarity selection pin 0: chip latch data at falling edge. 1: Chip latch data at rising edge. Fix it to IOVCC or VSSD level when only using system interface.
DDS	I	1	MPU	Selection the position of dummy line (321st line). 0: the end of the frame, 1: the beginning of the frame

Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
SDO	O	1	MPU	Serial bus interface data output pin. Keep it open while using parallel bus interface
CSTB	O	1	MPU	Frame synchronization signal output pin. Keep it open if not in use.
S1~S720	O	720	LCD	Source driver output pin. Output voltages to the liquid crystal.
G1~G321	O	321	LCD	Output signals to panel gate lines. VGH: the level to select the gate lines VGL: the level not to select the gate lines
VCOM1~4	O	4	LCD	VCOM output pin. They are short-circuited inside HX8312-A.

Input/Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
DB17-0	I/O	18	MPU	Operates liked an 18-bit bi-directional data bus. Fix it to IOVCC or VSSD level when using serial bus interface. Don't set MPU output as Hi-Z when MPU has no output.
OSC2-1	I/O	2	Oscillation Resistor	Connect an external resistor for generating internal clock by internal R-C oscillation. Or an external clock signal is supplied through OSC1 with OSC2 open.
C11A , C11B CX11A , CX11B	I/O	4	Step up Capacitor	Connect to the step-up capacitors for step up circuit 1 operation. Leave this pin open if the internal step-up circuit is not used.
C21A , C21B C22A , C22B C23A , C23B	I/O	6	Step up Capacitor	Connect to the step-up capacitors for step up circuit 2 operation. Leave this pin open if the internal step-up circuit is not used.
C12A , C12B	I/O	2	Step up Capacitor	Connect to the step-up capacitors for step up circuit 3 operation. Leave this pin open if the internal step-up circuit is not used.

Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
VCC	I	1	Power supply	A power supply for the internal logic circuit. VCC = 2.2 ~ 3.3V
VCI	I	1	Power supply	A Power supply for step-up circuit and power supply circuit. VCI = 2.5 ~ 3.3V
IOVCC	I	1	Power supply	Power supply for I/O circuit. IOVCC = 1.65 ~ 3.3V
V18	O	1	Bypass capacitor and VDDD, RVCC	1.8V regulator output. V18, VDDD and RVCC must have the same voltage level. Connect to VDDD and RVCC on the FPC.
RVCC	I	1	V18 and VDDD	Power supply for RAM circuit.
VDDD	I	1	V18 and RVCC	Power supply for logic circuit.
VSSD	I	1	System Ground	Ground for digital circuit.
VSSD2	I	1	System Ground	Ground for internal circuit.
VSSA	I	1	System Ground	Ground for analog circuit.
VGH	O	1	Bypass Capacitor	A positive power supply for the gate line drive circuit.
VGL	O	1	Bypass Capacitor Schottky Diode	A negative power supply for the gate line drive circuit. Insert a schottky diode in a forward direction to VSSA.
ADDVDH	I	1	DDVDH	Power supply pins for VS and COMH regulators. Connected to DDVDH on FPC
DDVDH	O	1	ADDVDH and Bypass Capacitor	Output supply pin. Connected to ADVDDH on FPC.
VCL	O	1	Bypass Capacitor	The voltage of Vci x (-1) output
VR2-1	O	2	Bypass Capacitor	Reference voltage output for the step-up circuit 2.
VS	O	1	Bypass Capacitor	Power supply for the source drive unit.
VGLDMY	O	1	-	A negative power supply for the gate line drive circuit.

Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
VCOMH	O	1	Bypass Capacitor	The high level voltage output of VCOM AC voltage output.
VCOML	O	1	Bypass Capacitor	The low level voltage output of VCOM AC voltage output. When VCOML is fixed to GND level (VCOMG=0), capacitor connection is not necessary.
VGS	I	1	GND or External R	A reference level for the grayscale voltage generating circuit.
VCOMR	I	1	Variable Resistor	Adjusting VCOMH level with an variable resistor between VDH and VSSA.
IOVCCDUM1~8	O	8	-	Pull-up pin for mode setting. These pins are connected to IOVCC inside the chip.
IOGNDDUM1~9	O	9	-	Pull-down pin for mode setting. These pins are connected to VSSD inside the chip.

Test Pin and Others				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
TEST2-1	I	2	GND	Test pin input. Must connect to VSSD.
DS1	O	1	-	Pin for gamma voltage output
VMON	O	1	-	Test pin output. Must be left open.
TESTA1, 2, 4	O	3	-	Test pin output. Must be left open.
THROUGH1	-	1	-	Dummy pads. Used to measure the COG contact resistance. THROUGH1 and THROUGH8 are short-circuited within the chip.
THROUGH8	-	1	-	
THROUGH2	-	1	-	Dummy pads. Used to measure the COG contact resistance. THROUGH2 and THROUGH7 are short-circuited within the chip.
THROUGH7	-	1	-	
THROUGH3	-	1	-	Dummy pads. Used to measure the COG contact resistance. THROUGH3 and THROUGH6 are short-circuited within the chip.
THROUGH6	-	1	-	
THROUGH4	-	1	-	Dummy pads. Used to measure the COG contact resistance. THROUGH4 and THROUGH5 are short-circuited within the chip.
THROUGH5	-	1	-	
DUMMYR1	-	1	-	Dummy pads. Used to measure the COG contact resistance. DUMMYR1 and DUMMYR2 are short-circuited within the chip.
DUMMYR2	-	1	-	
DUMMY 1-14, 16, 18, 20-50	-	47	-	Dummy pin. (There is no gold bumper on DUMMY 7,9,11, 23, 25 ,27)

Note : 1. The layout of VSSA , VSSD , VSSD2 need to be separated in panel, and short together in FPC.
2. The short connection of TEST1, TEST2 and VSSD must be located in FPC, not in panel.
3. Input pin must be fixed to VCC or VSSD when no use.
4. The output pin must be left floating when no use.
5. SDO is a output pin. It must be left floating when no use.
6. TEST2 , 1 are test pin inputs. It must be connected to VSSD
7. DS1, MON , TESTA1, 2, 4 are test pin outputs. It must be left floating.

PAD Coordinate

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	DUMMY1	-11928	-547.5	66	VGH	-9945	-701.5	131	VSYNC	-4420	-701.5	196	VDDD	1105	-701.5
2	DUMMY2	-11904	-702.5	67	VGH	-9860	-701.5	132	HSYNC	-4335	-701.5	197	VDDD	1190	-701.5
3	DUMMY3	-11880	-547.5	68	VGH	-9775	-701.5	133	HXYNC	-4250	-701.5	198	RVCC	1275	-701.5
4	DUMMY4	-11856	-702.5	69	VGH	-9690	-701.5	134	DOTCLK	-4165	-701.5	199	RVCC	1360	-701.5
5	DUMMY5	-11832	-547.5	70	C23A	-9605	-701.5	135	DOTCLK	-4080	-701.5	200	RVCC	1445	-701.5
6	DUMMY6	-11808	-702.5	71	C23A	-9520	-701.5	136	ENABLE	-3995	-701.5	201	RVCC	1530	-701.5
7	DUMMY7	-11784	-547.5	72	C23B	-9435	-701.5	137	ENABLE	-3910	-701.5	202	V18	1615	-701.5
8	DUMMY8	-11760	-702.5	73	C23B	-9350	-701.5	138	DB17	-3825	-701.5	203	V18	1700	-701.5
9	DUMMY9	-11736	-547.5	74	C22A	-9265	-701.5	139	DB17	-3740	-701.5	204	V18	1785	-701.5
10	DUMMY10	-11712	-702.5	75	C22A	-9180	-701.5	140	DB16	-3655	-701.5	205	V18	1870	-701.5
11	DUMMY11	-11688	-547.5	76	C22B	-9095	-701.5	141	DB16	-3570	-701.5	206	DUMMYR1	1955	-701.5
12	DUMMY12	-11664	-702.5	77	C22B	-9010	-701.5	142	DB15	-3485	-701.5	207	DUMMYR2	2040	-701.5
13	THROUGH1	-11640	-547.5	78	C21A	-8925	-701.5	143	DB15	-3400	-701.5	208	OSC1	2125	-701.5
14	THROUGH2	-11616	-702.5	79	C21A	-8840	-701.5	144	DB14	-3315	-701.5	209	OSC1	2210	-701.5
15	G278	-11592	-547.5	80	C21B	-8755	-701.5	145	DB14	-3230	-701.5	210	OSC2	2295	-701.5
16	G279	-11568	-702.5	81	C21B	-8670	-701.5	146	DB13	-3145	-701.5	211	OSC2	2380	-701.5
17	G280	-11544	-547.5	82	C12A	-8585	-701.5	147	DB13	-3060	-701.5	212	VSSD	2465	-701.5
18	G281	-11520	-702.5	83	C12A	-8500	-701.5	148	DB12	-2975	-701.5	213	VSSD	2550	-701.5
19	G282	-11496	-547.5	84	C12A	-8415	-701.5	149	DB12	-2890	-701.5	214	VSSD	2635	-701.5
20	G283	-11472	-702.5	85	C12A	-8330	-701.5	150	DB11	-2805	-701.5	215	VSSD	2720	-701.5
21	G284	-11448	-547.5	86	C12B	-8245	-701.5	151	DB11	-2720	-701.5	216	VSSD2	2805	-701.5
22	G285	-11424	-702.5	87	C12B	-8160	-701.5	152	DB10	-2635	-701.5	217	VSSD2	2890	-701.5
23	G286	-11400	-547.5	88	C12B	-8075	-701.5	153	DB10	-2550	-701.5	218	VSSD2	2975	-701.5
24	G287	-11376	-702.5	89	C12B	-7990	-701.5	154	DB9	-2465	-701.5	219	VSSD2	3060	-701.5
25	G288	-11352	-547.5	90	VR2	-7905	-701.5	155	DB9	-2380	-701.5	220	VSSA	3145	-701.5
26	G289	-11328	-702.5	91	VR2	-7820	-701.5	156	DB8	-2295	-701.5	221	VSSA	3230	-701.5
27	G290	-11304	-547.5	92	VR2	-7735	-701.5	157	DB8	-2210	-701.5	222	VSSA	3315	-701.5
28	G291	-11280	-702.5	93	VR2	-7650	-701.5	158	DB7	-2125	-701.5	223	VSSA	3400	-701.5
29	G292	-11256	-547.5	94	VGL	-7565	-701.5	159	DB7	-2040	-701.5	224	VSSA	3485	-701.5
30	G293	-11232	-702.5	95	VGL	-7480	-701.5	160	DB6	-1955	-701.5	225	VSSA	3570	-701.5
31	G294	-11208	-547.5	96	VGL	-7395	-701.5	161	DB6	-1870	-701.5	226	IOVCC	3655	-701.5
32	G295	-11184	-702.5	97	VGL	-7310	-701.5	162	DB5	-1785	-701.5	227	IOVCC	3740	-701.5
33	G296	-11160	-547.5	98	VGL	-7225	-701.5	163	DB5	-1700	-701.5	228	IOVCC	3825	-701.5
34	G297	-11136	-702.5	99	IOVCCDUM1	-7140	-701.5	164	DB4	-1615	-701.5	229	IOVCC	3910	-701.5
35	G298	-11112	-547.5	100	DDS	-7055	-701.5	165	DB4	-1530	-701.5	230	VCI	3995	-701.5
36	G299	-11088	-702.5	101	IOGNDDUM1	-6970	-701.5	166	DB3	-1445	-701.5	231	VCI	4080	-701.5
37	G300	-11064	-547.5	102	SCLEG1	-6885	-701.5	167	DB3	-1360	-701.5	232	VCI	4165	-701.5
38	G301	-11040	-702.5	103	IOVCCDUM2	-6800	-701.5	168	DB2	-1275	-701.5	233	VCI	4250	-701.5
39	G302	-11016	-547.5	104	SCLEG0	-6715	-701.5	169	DB2	-1190	-701.5	234	VCI	4335	-701.5
40	G303	-10992	-702.5	105	IOGNDDUM2	-6630	-701.5	170	DB1	-1105	-701.5	235	VCI	4420	-701.5
41	G304	-10968	-547.5	106	HSEG	-6545	-701.5	171	DB1	-1020	-701.5	236	VCC	4505	-701.5
42	G305	-10944	-702.5	107	IOVCCDUM3	-6460	-701.5	172	DB0	-935	-701.5	237	VCC	4590	-701.5
43	G306	-10920	-547.5	108	VSEG	-6375	-701.5	173	DB0	-850	-701.5	238	VCC	4675	-701.5
44	G307	-10896	-702.5	109	IOGNDDUM3	-6290	-701.5	174	NRD(E)	-765	-701.5	239	VCC	4760	-701.5
45	G308	-10872	-547.5	110	DCKEG	-6205	-701.5	175	NRD(E)	-680	-701.5	240	VGS	4845	-701.5
46	G309	-10848	-702.5	111	IOVCCDUM4	-6120	-701.5	176	NWR(RNW)	-595	-701.5	241	VGS	4930	-701.5
47	G310	-10824	-547.5	112	PSX	-6035	-701.5	177	NWR(RNW)	-510	-701.5	242	VCOMR	5015	-701.5
48	G311	-10800	-702.5	113	IOGNDDUM4	-5950	-701.5	178	RS	-425	-701.5	243	VCOMR	5100	-701.5
49	G312	-10776	-547.5	114	C86	-5865	-701.5	179	RS	-340	-701.5	244	VS	5185	-701.5
50	G313	-10752	-702.5	115	IOVCCDUM5	-5780	-701.5	180	SDO	-255	-701.5	245	VS	5270	-701.5
51	G314	-10728	-547.5	116	DTX1	-5695	-701.5	181	SDO	-170	-701.5	246	VS	5355	-701.5
52	G315	-10704	-702.5	117	IOGNDDUM5	-5610	-701.5	182	SDI	-85	-701.5	247	VS	5440	-701.5
53	G316	-10680	-547.5	118	DTX2	-5525	-701.5	183	SDI	0	-701.5	248	VCOML	5525	-701.5
54	G317	-10656	-702.5	119	IOVCCDUM6	-5440	-701.5	184	SCL	85	-701.5	249	VCOML	5610	-701.5
55	G318	-10632	-547.5	120	BWS0	-5355	-701.5	185	SCL	170	-701.5	250	VCOML	5695	-701.5
56	G319	-10608	-702.5	121	IOGNDDUM6	-5270	-701.5	186	NCS	255	-701.5	251	VCOML	5780	-701.5
57	G320	-10584	-547.5	122	BWS1	-5185	-701.5	187	NCS	340	-701.5	252	VCOMH	5865	-701.5
58	G321	-10560	-702.5	123	IOVCCDUM7	-5100	-701.5	188	CSTB	425	-701.5	253	VCOMH	5950	-701.5
59	DUMMY13	-10536	-547.5	124	BWS2	-5015	-701.5	189	CSTB	510	-701.5	254	VCOMH	6035	-701.5
60	DUMMY14	-10512	-702.5	125	IOGNDDUM7	-4930	-701.5	190	TEST1	595	-701.5	255	VCOMH	6120	-701.5
61	VMON	-10488	-547.5	126	RGBNCPU	-4845	-701.5	191	IOGNDDUM8	680	-701.5	256	VCL	6205	-701.5
62	DUMMY16	-10285	-701.5	127	IOVCCDUM8	-4760	-701.5	192	TEST2	765	-701.5	257	VCL	6290	-701.5
63	VCOM1	-10200	-701.5	128	NRESET	-4675	-701.5	193	IOGNDDUM9	850	-701.5	258	VCL	6375	-701.5
64	VCOM1	-10115	-701.5	129	NRESET	-4590	-701.5	194	VDDD	935	-701.5	259	VCL	6460	-701.5
65	DS1	-10030	-701.5	130	VSYNC	-4505	-701.5	195	VDDD	1020	-701.5	260	TESTA1	6545	-701.5

No.	Pad name	X	Y
261	TESTA1	6630	-701.5
262	VR1	6715	-701.5
263	VR1	6800	-701.5
264	VR1	6885	-701.5
265	VR1	6970	-701.5
266	ADDVDH	7055	-701.5
267	ADDVDH	7140	-701.5
268	ADDVDH	7225	-701.5
269	ADDVDH	7310	-701.5
270	DDVDH	7395	-701.5
271	DDVDH	7480	-701.5
272	DDVDH	7565	-701.5
273	DDVDH	7650	-701.5
274	CX11B	7735	-701.5
275	CX11B	7820	-701.5
276	CX11B	7905	-701.5
277	CX11B	7990	-701.5
278	CX11B	8075	-701.5
279	CX11B	8160	-701.5
280	CX11A	8245	-701.5
281	CX11A	8330	-701.5
282	CX11A	8415	-701.5
283	CX11A	8500	-701.5
284	CX11A	8585	-701.5
285	CX11A	8670	-701.5
286	C11B	8755	-701.5
287	C11B	8840	-701.5
288	C11B	8925	-701.5
289	C11B	9010	-701.5
290	C11B	9095	-701.5
291	C11B	9180	-701.5
292	C11A	9265	-701.5
293	C11A	9350	-701.5
294	C11A	9435	-701.5
295	C11A	9520	-701.5
296	C11A	9605	-701.5
297	C11A	9690	-701.5
298	TESTA2	9775	-701.5
299	DUMMY18	9860	-701.5
300	VCOM2	9945	-701.5
301	VCOM2	10030	-701.5
302	VCOM2	10115	-701.5
303	VCOM2	10200	-701.5
304	TESTA4	10285	-701.5
305	DUMMY20	10488	-547.5
306	DUMMY21	10512	-702.5
307	G1	10536	-547.5
308	G2	10560	-702.5
309	G3	10584	-547.5
310	G4	10608	-702.5
311	G5	10632	-547.5
312	G6	10656	-702.5
313	G7	10680	-547.5
314	G8	10704	-702.5
315	G9	10728	-547.5
316	G10	10752	-702.5
317	G11	10776	-547.5
318	G12	10800	-702.5
319	G13	10824	-547.5
320	G14	10848	-702.5
321	G15	10872	-547.5
322	G16	10896	-702.5
323	G17	10920	-547.5
324	G18	10944	-702.5
325	G19	10968	-547.5
326	G20	10992	-702.5
327	G21	11016	-547.5
328	G22	11040	-702.5
329	G23	11064	-547.5
330	G24	11088	-702.5
331	G25	11112	-547.5
332	G26	11136	-702.5
333	G27	11160	-547.5
334	G28	11184	-702.5
335	G29	11208	-547.5
336	G30	11232	-702.5
337	G31	11256	-547.5
338	G32	11280	-702.5
339	G33	11304	-547.5
340	G34	11328	-702.5
341	G35	11352	-547.5
342	G36	11376	-702.5
343	G37	11400	-547.5
344	G38	11424	-702.5
345	G39	11448	-547.5
346	G40	11472	-702.5
347	G41	11496	-547.5
348	G42	11520	-702.5
349	G43	11544	-547.5
350	G44	11568	-702.5
351	G45	11592	-547.5
352	THROUGH3	11616	-702.5
353	THROUGH4	11640	-547.5
354	DUMMY22	11664	-702.5
355	DUMMY23	11688	-547.5
356	DUMMY24	11712	-702.5
357	DUMMY25	11736	-547.5
358	DUMMY26	11760	-702.5
359	DUMMY27	11784	-547.5
360	DUMMY28	11808	-702.5
361	DUMMY29	11832	-547.5
362	DUMMY30	11856	-702.5
363	DUMMY31	11880	-547.5
364	DUMMY32	11904	-702.5
365	DUMMY33	11928	-547.5
366	DUMMY34	11736	702.5
367	VGLDMY	11712	547.5
368	DUMMY35	11688	702.5
369	DUMMY36	11664	547.5
370	THROUGH5	11640	702.5
371	THROUGH6	11616	547.5
372	G46	11592	702.5
373	G47	11568	547.5
374	G48	11544	702.5
375	G49	11520	547.5
376	G50	11496	702.5
377	G51	11472	547.5
378	G52	11448	702.5
379	G53	11424	547.5
380	G54	11400	702.5
381	G55	11376	547.5
382	G56	11352	702.5
383	G57	11328	547.5
384	G58	11304	702.5
385	G59	11280	547.5
386	G60	11256	702.5
387	G61	11232	547.5
388	G62	11208	702.5
389	G63	11184	547.5
390	G64	11160	702.5
391	G65	11136	547.5
392	G66	11112	702.5
393	G67	11088	547.5
394	G68	11064	702.5
395	G69	11040	547.5
396	G70	11016	702.5
397	G71	10992	547.5
398	G72	10968	702.5
399	G73	10944	547.5
400	G74	10920	702.5
401	G75	10896	547.5
402	G76	10872	702.5
403	G77	10848	547.5
404	G78	10824	702.5
405	G79	10800	547.5
406	G80	10776	702.5
407	G81	10752	547.5
408	G82	10728	702.5
409	G83	10704	547.5
410	G84	10680	702.5
411	G85	10656	547.5
412	G86	10632	702.5
413	G87	10608	547.5
414	G88	10584	702.5
415	G89	10560	547.5
416	G90	10536	702.5
417	G91	10512	547.5
418	G92	10488	702.5
419	G93	10464	547.5
420	G94	10440	702.5
421	G95	10416	547.5
422	G96	10392	702.5
423	G97	10368	547.5
424	G98	10344	702.5
425	G99	10320	547.5
426	G100	10296	702.5
427	G101	10272	547.5
428	G102	10248	702.5
429	G103	10224	547.5
430	G104	10200	702.5
431	G105	10176	547.5
432	G106	10152	702.5
433	G107	10128	547.5
434	G108	10104	702.5
435	G109	10080	547.5
436	G110	10056	702.5
437	G111	10032	547.5
438	G112	10008	702.5
439	G113	9984	547.5
440	G114	9960	702.5
441	G115	9936	547.5
442	G116	9912	702.5
443	G117	9888	547.5
444	G118	9864	702.5
445	G119	9840	547.5
446	G120	9816	702.5
447	G121	9792	547.5
448	G122	9768	702.5
449	G123	9744	547.5
450	G124	9720	702.5
451	G125	9696	547.5
452	G126	9672	702.5
453	G127	9648	547.5
454	G128	9624	702.5
455	G129	9600	547.5
456	G130	9576	702.5
457	G131	9552	547.5
458	G132	9528	702.5
459	G133	9504	547.5
460	G134	9480	702.5
461	G135	9456	547.5
462	G136	9432	702.5
463	G137	9408	547.5
464	G138	9384	702.5
465	G139	9360	547.5
466	G140	9336	702.5
467	G141	9312	547.5
468	G142	9288	702.5
469	G143	9264	547.5
470	G144	9240	702.5
471	G145	9216	547.5
472	G146	9192	702.5
473	G148	9168	547.5
474	G148	9144	702.5
475	G149	9120	547.5
476	G150	9096	702.5
477	G151	9072	547.5
478	G152	9048	702.5
479	G153	9024	547.5
480	G154	9000	702.5
481	G155	8976	547.5
482	G156	8952	702.5
483	G157	8928	547.5
484	G158	8904	702.5
485	G159	8880	547.5
486	G160	8856	702.5
487	G161	8832	547.5
488	DUMMY37	8808	702.5
489	DUMMY38	8784	547.5
490	VCOM3	8760	702.5
491	VCOM3	8736	547.5
492	DUMMY39	8712	702.5
493	DUMMY40	8688	547.5
494	DUMMY41	8664	702.5
495	S720	8640	547.5
496	S719	8616	702.5
497	S718	8592	547.5
498	S717	8568	702.5
499	S716	8544	547.5
500	S715	8520	702.5
501	S714	8496	547.5
502	S713	8472	702.5
503	S712	8448	547.5
504	S711	8424	702.5
505	S710	8400	547.5
506	S709	8376	702.5
507	S708	8352	547.5
508	S707	8328	702.5
509	S706	8304	547.5
510	S705	8280	702.5
511	S704	8256	547.5
512	S703	8232	702.5
513	S702	8208	547.5
514	S701	8184	702.5
515	S700	8160	547.5
516	S699	8136	702.5
517	S698	8112	547.5
518	S697	8088	702.5
519	S696	8064	547.5
520	S695	8040	702.5

No.	Pad name	X	Y
521	S694	8016	547.5
522	S693	7992	702.5
523	S692	7968	547.5
524	S691	7944	702.5
525	S690	7920	547.5
526	S689	7896	702.5
527	S688	7872	547.5
528	S687	7848	702.5
529	S686	7824	547.5
530	S685	7800	702.5
531	S684	7776	547.5
532	S683	7752	702.5
533	S682	7728	547.5
534	S681	7704	702.5
535	S680	7680	547.5
536	S679	7656	702.5
537	S678	7632	547.5
538	S677	7608	702.5
539	S676	7584	547.5
540	S675	7560	702.5
541	S674	7536	547.5
542	S673	7512	702.5
543	S672	7488	547.5
544	S671	7464	702.5
545	S670	7440	547.5
546	S669	7416	702.5
547	S668	7392	547.5
548	S667	7368	702.5
549	S666	7344	547.5
550	S665	7320	702.5
551	S664	7296	547.5
552	S663	7272	702.5
553	S662	7248	547.5
554	S661	7224	702.5
555	S660	7200	547.5
556	S659	7176	702.5
557	S658	7152	547.5
558	S657	7128	702.5
559	S656	7104	547.5
560	S655	7080	702.5
561	S654	7056	547.5
562	S653	7032	702.5
563	S652	7008	547.5
564	S651	6984	702.5
565	S650	6960	547.5
566	S649	6936	702.5
567	S648	6912	547.5
568	S647	6888	702.5
569	S646	6864	547.5
570	S645	6840	702.5
571	S644	6816	547.5
572	S643	6792	702.5
573	S642	6768	547.5
574	S641	6744	702.5
575	S640	6720	547.5
576	S639	6696	702.5
577	S638	6672	547.5
578	S637	6648	702.5
579	S636	6624	547.5
580	S635	6600	702.5
581	S634	6576	547.5
582	S633	6552	702.5
583	S632	6528	547.5
584	S631	6504	702.5
585	S630	6480	547.5
586	S629	6456	702.5
587	S628	6432	547.5
588	S627	6408	702.5
589	S626	6384	547.5
590	S625	6360	702.5
591	S624	6336	547.5
592	S623	6312	702.5
593	S622	6288	547.5
594	S621	6264	702.5
595	S620	6240	547.5
596	S619	6216	702.5
597	S618	6192	547.5
598	S617	6168	702.5
599	S616	6144	547.5
600	S615	6120	702.5
601	S614	6096	547.5
602	S613	6072	702.5
603	S612	6048	547.5
604	S611	6024	702.5
605	S610	6000	547.5
606	S609	5976	702.5
607	S608	5952	547.5
608	S607	5928	702.5
609	S606	5904	547.5
610	S605	5880	702.5
611	S604	5856	547.5
612	S603	5832	702.5
613	S602	5808	547.5
614	S601	5784	702.5
615	S600	5760	547.5
616	S599	5736	702.5
617	S598	5712	547.5
618	S597	5688	702.5
619	S596	5664	547.5
620	S595	5640	702.5
621	S594	5616	547.5
622	S593	5592	702.5
623	S592	5568	547.5
624	S591	5544	702.5
625	S590	5520	547.5
626	S589	5496	702.5
627	S588	5472	547.5
628	S587	5448	702.5
629	S586	5424	547.5
630	S585	5400	702.5
631	S584	5376	547.5
632	S583	5352	702.5
633	S582	5328	547.5
634	S581	5304	702.5
635	S580	5280	547.5
636	S579	5256	702.5
637	S578	5232	547.5
638	S577	5208	702.5
639	S576	5184	547.5
640	S575	5160	702.5
641	S574	5136	547.5
642	S573	5112	702.5
643	S572	5088	547.5
644	S571	5064	702.5
645	S570	5040	547.5
646	S569	5016	702.5
647	S568	4992	547.5
648	S567	4968	702.5
649	S566	4944	547.5
650	S565	4920	702.5
651	S564	4896	547.5
652	S563	4872	702.5
653	S562	4848	547.5
654	S561	4824	702.5
655	S560	4800	547.5
656	S559	4776	702.5
657	S558	4752	547.5
658	S557	4728	702.5
659	S556	4704	547.5
660	S555	4680	702.5
661	S554	4656	547.5
662	S553	4632	702.5
663	S552	4608	547.5
664	S551	4584	702.5
665	S550	4560	547.5
666	S549	4536	702.5
667	S548	4512	547.5
668	S547	4488	702.5
669	S546	4464	547.5
670	S545	4440	702.5
671	S544	4416	547.5
672	S543	4392	702.5
673	S542	4368	547.5
674	S541	4344	702.5
675	S540	4320	547.5
676	S539	4296	702.5
677	S538	4272	547.5
678	S537	4248	702.5
679	S536	4224	547.5
680	S535	4200	702.5
681	S534	4176	547.5
682	S533	4152	702.5
683	S532	4128	547.5
684	S531	4104	702.5
685	S530	4080	547.5
686	S529	4056	702.5
687	S528	4032	547.5
688	S527	4008	702.5
689	S526	3984	547.5
690	S525	3960	702.5
691	S524	3936	547.5
692	S523	3912	702.5
693	S522	3888	547.5
694	S521	3864	702.5
695	S520	3840	547.5
696	S519	3816	702.5
697	S518	3792	547.5
698	S517	3768	702.5
699	S516	3744	547.5
700	S515	3720	702.5
701	S514	3696	547.5
702	S513	3672	702.5
703	S512	3648	547.5
704	S511	3624	702.5
705	S510	3600	547.5
706	S509	3576	702.5
707	S508	3552	547.5
708	S507	3528	702.5
709	S506	3504	547.5
710	S505	3480	702.5
711	S504	3456	547.5
712	S503	3432	702.5
713	S502	3408	547.5
714	S501	3384	702.5
715	S500	3360	547.5
716	S499	3336	702.5
717	S498	3312	547.5
718	S497	3288	702.5
719	S496	3264	547.5
720	S495	3240	702.5
721	S494	3216	547.5
722	S493	3192	702.5
723	S492	3168	547.5
724	S491	3144	702.5
725	S490	3120	547.5
726	S489	3096	702.5
727	S488	3072	547.5
728	S487	3048	702.5
729	S486	3024	547.5
730	S485	3000	702.5
731	S484	2976	547.5
732	S483	2952	702.5
733	S482	2928	547.5
734	S481	2904	702.5
735	S480	2880	547.5
736	S479	2856	702.5
737	S478	2832	547.5
738	S477	2808	702.5
739	S476	2784	547.5
740	S475	2760	702.5
741	S474	2736	547.5
742	S473	2712	702.5
743	S472	2688	547.5
744	S471	2664	702.5
745	S470	2640	547.5
746	S469	2616	702.5
747	S468	2592	547.5
748	S467	2568	702.5
749	S466	2544	547.5
750	S465	2520	702.5
751	S464	2496	547.5
752	S463	2472	702.5
753	S462	2448	547.5
754	S461	2424	702.5
755	S460	2400	547.5
756	S459	2376	702.5
757	S458	2352	547.5
758	S457	2328	702.5
759	S456	2304	547.5
760	S455	2280	702.5
761	S454	2256	547.5
762	S453	2232	702.5
763	S452	2208	547.5
764	S451	2184	702.5
765	S450	2160	547.5
766	S449	2136	702.5
767	S448	2112	547.5
768	S447	2088	702.5
769	S446	2064	547.5
770	S445	2040	702.5
771	S444	2016	547.5
772	S443	1992	702.5
773	S442	1968	547.5
774	S441	1944	702.5
775	S440	1920	547.5
776	S439	1896	702.5
777	S438	1872	547.5
778	S437	1848	702.5
779	S436	1824	547.5
780	S435	1800	702.5

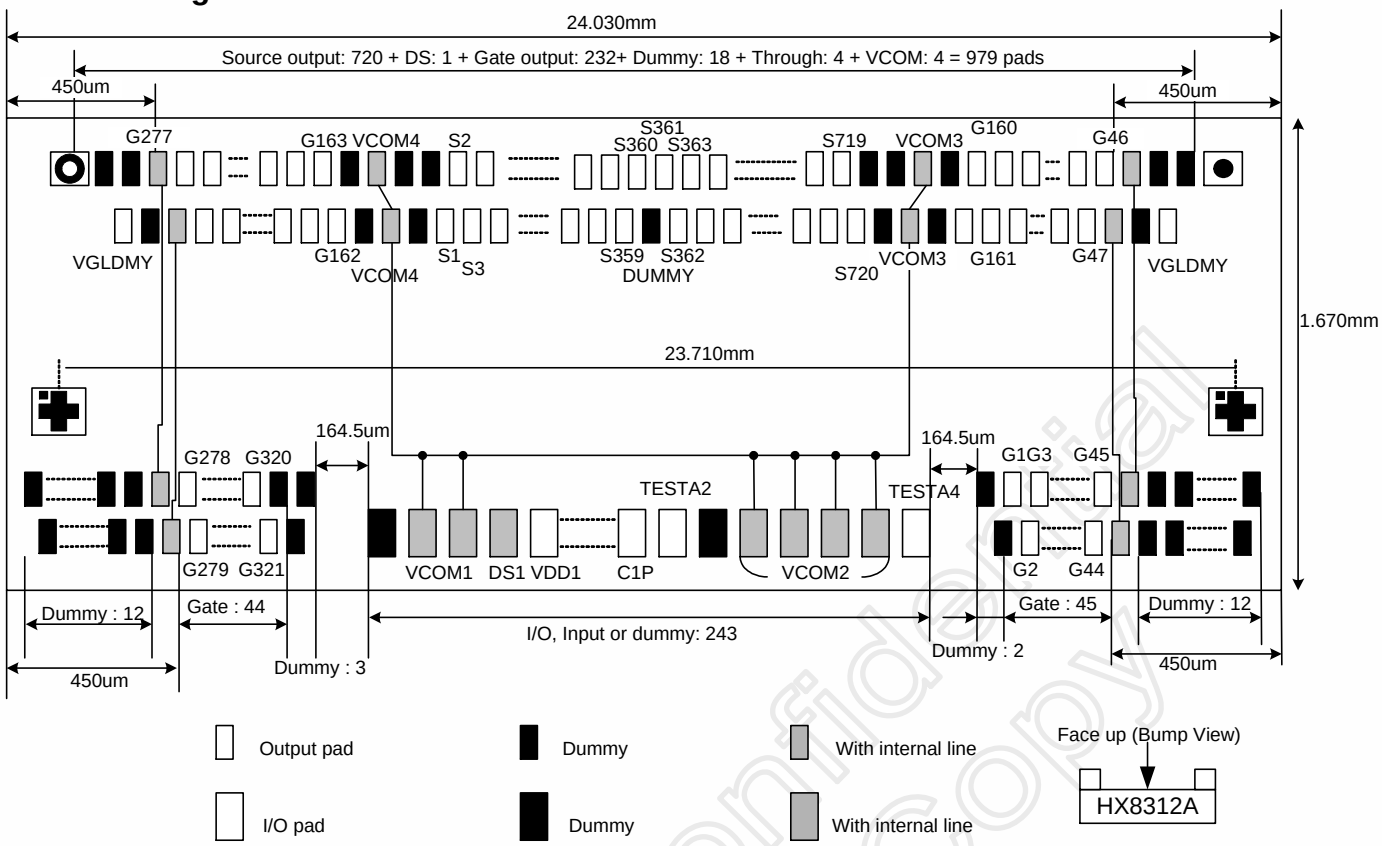
No.	Pad name	X	Y
781	S434	1776	547.5
782	S433	1752	702.5
783	S432	1728	547.5
784	S431	1704	702.5
785	S430	1680	547.5
786	S429	1656	702.5
787	S428	1632	547.5
788	S427	1608	702.5
789	S426	1584	547.5
790	S425	1560	702.5
791	S424	1536	547.5
792	S423	1512	702.5
793	S422	1488	547.5
794	S421	1464	702.5
795	S420	1440	547.5
796	S419	1416	702.5
797	S418	1392	547.5
798	S417	1368	702.5
799	S416	1344	547.5
800	S415	1320	702.5
801	S414	1296	547.5
802	S413	1272	702.5
803	S412	1248	547.5
804	S411	1224	702.5
805	S410	1200	547.5
806	S409	1176	702.5
807	S408	1152	547.5
808	S407	1128	702.5
809	S406	1104	547.5
810	S405	1080	702.5
811	S404	1056	547.5
812	S403	1032	702.5
813	S402	1008	547.5
814	S401	984	702.5
815	S400	960	547.5
816	S399	936	702.5
817	S398	912	547.5
818	S397	888	702.5
819	S396	864	547.5
820	S395	840	702.5
821	S394	816	547.5
822	S393	792	702.5
823	S392	768	547.5
824	S391	744	702.5
825	S390	720	547.5
826	S389	696	702.5
827	S388	672	547.5
828	S387	648	702.5
829	S386	624	547.5
830	S385	600	702.5
831	S384	576	547.5
832	S383	552	702.5
833	S382	528	547.5
834	S381	504	702.5
835	S380	480	547.5
836	S379	456	702.5
837	S378	432	547.5
838	S377	408	702.5
839	S376	384	547.5
840	S375	360	702.5
841	S374	336	547.5
842	S373	312	702.5
843	S372	288	547.5
844	S371	264	702.5
845	S370	240	547.5
846	S369	216	702.5
847	S368	192	547.5
848	S367	168	702.5
849	S366	144	547.5
850	S365	120	702.5
851	S364	96	547.5
852	S363	72	702.5
853	S362	48	547.5
854	S361	24	702.5
855	DUMMY42	0	547.5
856	S360	-24	702.5
857	S359	-48	547.5
858	S358	-72	702.5
859	S357	-96	547.5
860	S356	-120	702.5
861	S355	-144	547.5
862	S354	-168	702.5
863	S353	-192	547.5
864	S352	-216	702.5
865	S351	-240	547.5
866	S350	-264	702.5
867	S349	-288	547.5
868	S348	-312	702.5
869	S347	-336	547.5
870	S346	-360	702.5
871	S345	-384	547.5
872	S344	-408	702.5
873	S343	-432	547.5
874	S342	-456	702.5
875	S341	-480	547.5
876	S340	-504	702.5
877	S339	-528	547.5
878	S338	-552	702.5
879	S337	-576	547.5
880	S336	-600	702.5
881	S335	-624	547.5
882	S334	-648	702.5
883	S333	-672	547.5
884	S332	-696	702.5
885	S331	-720	547.5
886	S330	-744	702.5
887	S329	-768	547.5
888	S328	-792	702.5
889	S327	-816	547.5
890	S326	-840	702.5
891	S325	-864	547.5
892	S224	-888	702.5
893	S223	-912	547.5
894	S322	-936	702.5
895	S321	-960	547.5
896	S320	-984	702.5
897	S319	-1008	547.5
898	S318	-1032	702.5
899	S317	-1056	547.5
900	S316	-1080	702.5
901	S315	-1104	547.5
902	S314	-1128	702.5
903	S313	-1152	547.5
904	S312	-1176	702.5
905	S311	-1200	547.5
906	S310	-1224	702.5
907	S309	-1248	547.5
908	S308	-1272	702.5
909	S307	-1296	547.5
910	S306	-1320	702.5
911	S305	-1344	547.5
912	S304	-1368	702.5
913	S303	-1392	547.5
914	S302	-1416	702.5
915	S301	-1440	547.5
916	S300	-1464	702.5
917	S299	-1488	547.5
918	S298	-1512	702.5
919	S297	-1536	547.5
920	S296	-1560	702.5
921	S295	-1584	547.5
922	S294	-1608	702.5
923	S293	-1632	547.5
924	S292	-1656	702.5
925	S291	-1680	547.5
926	S290	-1704	702.5
927	S289	-1728	547.5
928	S288	-1752	702.5
929	S287	-1776	547.5
930	S286	-1800	702.5
931	S285	-1824	547.5
932	S284	-1848	702.5
933	S283	-1872	547.5
934	S282	-1896	702.5
935	S281	-1920	547.5
936	S280	-1944	702.5
937	S279	-1968	547.5
938	S278	-1992	702.5
939	S277	-2016	547.5
940	S276	-2040	702.5
941	S275	-2064	547.5
942	S274	-2088	702.5
943	S273	-2112	547.5
944	S272	-2136	702.5
945	S271	-2160	547.5
946	S270	-2184	702.5
947	S269	-2208	547.5
948	S268	-2232	702.5
949	S267	-2256	547.5
950	S266	-2280	702.5
951	S265	-2304	547.5
952	S264	-2328	702.5
953	S263	-2352	547.5
954	S262	-2376	702.5
955	S261	-2400	547.5
956	S260	-2424	702.5
957	S259	-2448	547.5
958	S258	-2472	702.5
959	S257	-2496	547.5
960	S256	-2520	702.5
961	S255	-2544	547.5
962	S254	-2568	702.5
963	S253	-2592	547.5
964	S252	-2616	702.5
965	S251	-2640	547.5
966	S250	-2664	702.5
967	S249	-2688	547.5
968	S248	-2712	702.5
969	S247	-2736	547.5
970	S246	-2760	702.5
971	S245	-2784	547.5
972	S244	-2808	702.5
973	S243	-2832	547.5
974	S242	-2856	702.5
975	S241	-2880	547.5
976	S240	-2904	702.5
977	S239	-2928	547.5
978	S238	-2952	702.5
979	S237	-2976	547.5
980	S236	-3000	702.5
981	S235	-3024	547.5
982	S234	-3048	702.5
983	S233	-3072	547.5
984	S232	-3096	702.5
985	S231	-3120	547.5
986	S230	-3144	702.5
987	S229	-3168	547.5
988	S228	-3192	702.5
989	S227	-3216	547.5
990	S226	-3240	702.5
991	S225	-3264	547.5
992	S224	-3288	702.5
993	S223	-3312	547.5
994	S222	-3336	702.5
995	S221	-3360	547.5
996	S220	-3384	702.5
997	S219	-3408	547.5
998	S218	-3432	702.5
999	S217	-3456	547.5
1000	S216	-3480	702.5
1001	S215	-3504	547.5
1002	S214	-3528	702.5
1003	S213	-3552	547.5
1004	S212	-3576	702.5
1005	S211	-3600	547.5
1006	S210	-3624	702.5
1007	S209	-3648	547.5
1008	S208	-3672	702.5
1009	S207	-3696	547.5
1010	S206	-3720	702.5
1011	S205	-3744	547.5
1012	S204	-3768	702.5
1013	S203	-3792	547.5
1014	S202	-3816	702.5
1015	S201	-3840	547.5
1016	S200	-3864	702.5
1017	S199	-3888	547.5
1018	S198	-3912	702.5
1019	S197	-3936	547.5
1020	S196	-3960	702.5
1021	S195	-3984	547.5
1022	S194	-4008	702.5
1023	S193	-4032	547.5
1024	S192	-4056	702.5
1025	S191	-4080	547.5
1026	S190	-4104	702.5
1027	S189	-4128	547.5
1028	S188	-4152	702.5
1029	S187	-4176	547.5
1030	S186	-4200	702.5
1031	S185	-4224	547.5
1032	S184	-4248	702.5
1033	S183	-4272	547.5
1034	S182	-4296	702.5
1035	S181	-4320	547.5
1036	S180	-4344	702.5
1037	S179	-4368	547.5
1038	S178	-4392	702.5
1039	S177	-4416	547.5
1040	S176	-4440	702.5

No.	Pad name	X	Y
1041	S175	-4464	547.5
1042	S174	-4488	702.5
1043	S173	-4512	547.5
1044	S172	-4536	702.5
1045	S171	-4560	547.5
1046	S170	-4584	702.5
1047	S169	-4608	547.5
1048	S168	-4632	702.5
1049	S167	-4656	547.5
1050	S166	-4680	702.5
1051	S165	-4704	547.5
1052	S164	-4728	702.5
1053	S163	-4752	547.5
1054	S162	-4776	702.5
1055	S161	-4800	547.5
1056	S160	-4824	702.5
1057	S159	-4848	547.5
1058	S158	-4872	702.5
1059	S157	-4896	547.5
1060	S156	-4920	702.5
1061	S155	-4944	547.5
1062	S154	-4968	702.5
1063	S153	-4992	547.5
1064	S152	-5016	702.5
1065	S151	-5040	547.5
1066	S150	-5064	702.5
1067	S149	-5088	547.5
1068	S148	-5112	702.5
1069	S147	-5136	547.5
1070	S146	-5160	702.5
1071	S145	-5184	547.5
1072	S144	-5208	702.5
1073	S143	-5232	547.5
1074	S142	-5256	702.5
1075	S141	-5280	547.5
1076	S140	-5304	702.5
1077	S139	-5328	547.5
1078	S138	-5352	702.5
1079	S137	-5376	547.5
1080	S136	-5400	702.5
1081	S135	-5424	547.5
1082	S134	-5448	702.5
1083	S133	-5472	547.5
1084	S132	-5496	702.5
1085	S131	-5520	547.5
1086	S130	-5544	702.5
1087	S129	-5568	547.5
1088	S128	-5592	702.5
1089	S127	-5616	547.5
1090	S126	-5640	702.5
1091	S125	-5664	547.5
1092	S124	-5688	702.5
1093	S123	-5712	547.5
1094	S122	-5736	702.5
1095	S121	-5760	547.5
1096	S120	-5784	702.5
1097	S119	-5808	547.5
1098	S118	-5832	702.5
1099	S117	-5856	547.5
1100	S116	-5880	702.5
1101	S115	-5904	547.5
1102	S114	-5928	702.5
1103	S113	-5952	547.5
1104	S112	-5976	702.5
1105	S111	-6000	547.5
1106	S110	-6024	702.5
1107	S109	-6048	547.5
1108	S108	-6072	702.5
1109	S107	-6096	547.5
1110	S106	-6120	702.5
1111	S105	-6144	547.5
1112	S104	-6168	702.5
1113	S103	-6192	547.5
1114	S102	-6216	702.5
1115	S101	-6240	547.5
1116	S100	-6264	702.5
1117	S99	-6288	547.5
1118	S98	-6312	702.5
1119	S97	-6336	547.5
1120	S96	-6360	702.5
1121	S95	-6384	547.5
1122	S94	-6408	702.5
1123	S93	-6432	547.5
1124	S92	-6456	702.5
1125	S91	-6480	547.5
1126	S90	-6504	702.5
1127	S89	-6528	547.5
1128	S88	-6552	702.5
1129	S87	-6576	547.5
1130	S86	-6600	702.5
1131	S85	-6624	547.5
1132	S84	-6648	702.5
1133	S83	-6672	547.5
1134	S82	-6696	702.5
1135	S81	-6720	547.5
1136	S80	-6744	702.5
1137	S79	-6768	547.5
1138	S78	-6792	702.5
1139	S77	-6816	547.5
1140	S76	-6840	702.5
1141	S75	-6864	547.5
1142	S74	-6888	702.5
1143	S73	-6912	547.5
1144	S72	-6936	702.5
1145	S71	-6960	547.5
1146	S70	-6984	702.5
1147	S69	-7008	547.5
1148	S68	-7032	702.5
1149	S67	-7056	547.5
1150	S66	-7080	702.5
1151	S65	-7104	547.5
1152	S64	-7128	702.5
1153	S63	-7152	547.5
1154	S62	-7176	702.5
1155	S61	-7200	547.5
1156	S60	-7224	702.5
1157	S59	-7248	547.5
1158	S58	-7272	702.5
1159	S57	-7296	547.5
1160	S56	-7320	702.5
1161	S55	-7344	547.5
1162	S54	-7368	702.5
1163	S53	-7392	547.5
1164	S52	-7416	702.5
1165	S51	-7440	547.5
1166	S50	-7464	702.5
1167	S49	-7488	547.5
1168	S48	-7512	702.5
1169	S47	-7536	547.5
1170	S46	-7560	702.5
1171	S45	-7584	547.5
1172	S44	-7608	702.5
1173	S43	-7632	547.5
1174	S42	-7656	702.5
1175	S41	-7680	547.5
1176	S40	-7704	702.5
1177	S39	-7728	547.5
1178	S38	-7752	702.5
1179	S37	-7776	547.5
1180	S36	-7800	702.5
1181	S35	-7824	547.5
1182	S34	-7848	702.5
1183	S33	-7872	547.5
1184	S32	-7896	702.5
1185	S31	-7920	547.5
1186	S30	-7944	702.5
1187	S29	-7968	547.5
1188	S28	-7992	702.5
1189	S27	-8016	547.5
1190	S26	-8040	702.5
1191	S25	-8064	547.5
1192	S24	-8088	702.5
1193	S23	-8112	547.5
1194	S22	-8136	702.5
1195	S21	-8160	547.5
1196	S20	-8184	702.5
1197	S19	-8208	547.5
1198	S18	-8232	702.5
1199	S17	-8256	547.5
1200	S16	-8280	702.5
1201	S15	-8304	547.5
1202	S14	-8328	702.5
1203	S13	-8352	547.5
1204	S12	-8376	702.5
1205	S11	-8400	547.5
1206	S10	-8424	702.5
1207	S9	-8448	547.5
1208	S8	-8472	702.5
1209	S7	-8496	547.5
1210	S6	-8520	702.5
1211	S5	-8544	547.5
1212	S4	-8568	702.5
1213	S3	-8592	547.5
1214	S2	-8616	702.5
1215	S1	-8640	547.5
1216	DUMMY43	-8664	702.5
1217	DUMMY44	-8688	547.5
1218	DUMMY45	-8712	702.5
1219	VCOM4	-8736	547.5
1220	VCOM4	-8760	702.5
1221	DUMMY46	-8784	547.5
1222	DUMMY47	-8808	702.5
1223	G162	-8832	547.5
1224	G163	-8856	702.5
1225	G164	-8880	547.5
1226	G165	-8904	702.5
1227	G166	-8928	547.5
1228	G167	-8952	702.5
1229	G168	-8976	547.5
1230	G169	-9000	702.5
1231	G170	-9024	547.5
1232	G171	-9048	702.5
1233	G172	-9072	547.5
1234	G173	-9096	702.5
1235	G174	-9120	547.5
1236	G175	-9144	702.5
1237	G176	-9168	547.5
1238	G177	-9192	702.5
1239	G178	-9216	547.5
1240	G179	-9240	702.5
1241	G180	-9264	547.5
1242	G181	-9288	702.5
1243	G182	-9312	547.5
1244	G183	-9336	702.5
1245	G184	-9360	547.5
1246	G185	-9384	702.5
1247	G186	-9408	547.5
1248	G187	-9432	702.5
1249	G188	-9456	547.5
1250	G189	-9480	702.5
1251	G190	-9504	547.5
1252	G191	-9528	702.5
1253	G192	-9552	547.5
1254	G193	-9576	702.5
1255	G194	-9600	547.5
1256	G195	-9624	702.5
1257	G196	-9648	547.5
1258	G197	-9672	702.5
1259	G198	-9696	547.5
1260	G199	-9720	702.5
1261	G200	-9744	547.5
1262	G201	-9768	702.5
1263	G202	-9792	547.5
1264	G203	-9816	702.5
1265	G204	-9840	547.5
1266	G205	-9864	702.5
1267	G206	-9888	547.5
1268	G207	-9912	702.5
1269	G208	-9936	547.5
1270	G209	-9960	702.5
1271	G210	-9984	547.5
1272	G211	-10008	702.5
1273	G212	-10032	547.5
1274	G213	-10056	702.5
1275	G214	-10080	547.5
1276	G215	-10104	702.5
1277	G216	-10128	547.5
1278	G217	-10152	702.5
1279	G218	-10176	547.5
1280	G219	-10200	702.5
1281	G220	-10224	547.5
1282	G221	-10248	702.5
1283	G222	-10272	547.5
1284	G223	-10296	702.5
1285	G224	-10320	547.5
1286	G225	-10344	702.5
1287	G226	-10368	547.5
1288	G227	-10392	702.5
1289	G228	-10416	547.5
1290	G229	-10440	702.5
1291	G230	-10464	547.5
1292	G231	-10488	702.5
1293	G232	-10512	547.5
1294	G233	-10536	702.5
1295	G234	-10560	547.5
1296	G235	-10584	702.5
1297	G236	-10608	547.5
1298	G237	-10632	702.5
1299	G238	-10656	547.5
1300	G239	-10680	702.5

No.	Pad name	X	Y
1301	G240	-10704	547.5
1302	G241	-10728	702.5
1303	G242	-10752	547.5
1304	G243	-10776	702.5
1305	G244	-10800	547.5
1306	G245	-10824	702.5
1307	G246	-10848	547.5
1308	G247	-10872	702.5
1309	G248	-10896	547.5
1310	G249	-10920	702.5
1311	G250	-10944	547.5
1312	G251	-10968	702.5
1313	G252	-10992	547.5
1314	G253	-11016	702.5
1315	G254	-11040	547.5
1316	G255	-11064	702.5
1317	G256	-11088	547.5
1318	G257	-11112	702.5
1319	G258	-11136	547.5
1320	G259	-11160	702.5
1321	G260	-11184	547.5
1322	G261	-11208	702.5
1323	G262	-11232	547.5
1324	G263	-11256	702.5
1325	G264	-11280	547.5
1326	G265	-11304	702.5
1327	G266	-11328	547.5
1328	G267	-11352	702.5
1329	G268	-11376	547.5
1330	G269	-11400	702.5
1331	G270	-11424	547.5
1332	G271	-11448	702.5
1333	G272	-11472	547.5
1334	G273	-11496	702.5
1335	G274	-11520	547.5
1336	G275	-11544	702.5
1337	G276	-11568	547.5
1338	G277	-11592	702.5
1339	THROUGH7	-11616	547.5
1340	THROUGH8	-11640	702.5
1341	DUMMY48	-11664	547.5
1342	DUMMY49	-11688	702.5
1343	VGLDMY	-11712	547.5
1344	DUMMY50	-11736	702.5

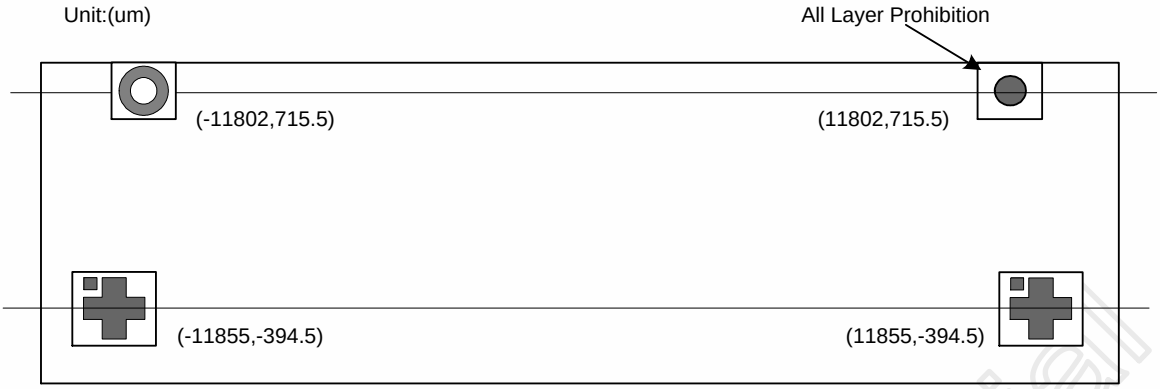
Alignment mark	X	Y
(1-a)	-11855	-394.5
(1-b)	11855	-394.5
(2-a)	-11802	715.5
(2-b)	11802	715.5

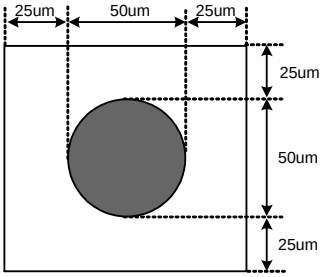
BUMP Arrangement

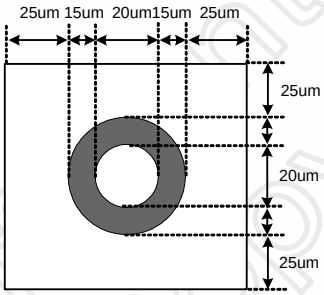


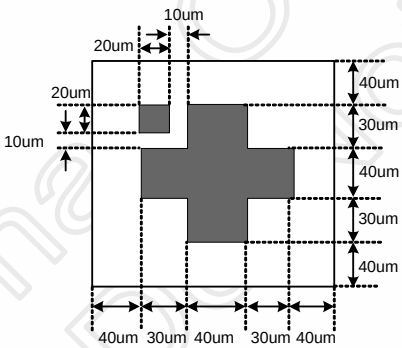
Note: There is no gold bumper on DUMMY 7,9,11, 23, 25, 27 pins.

Alignment mark



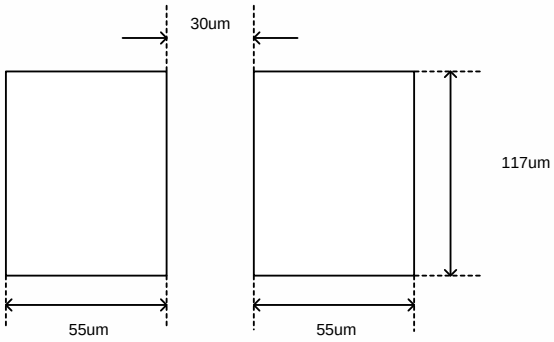




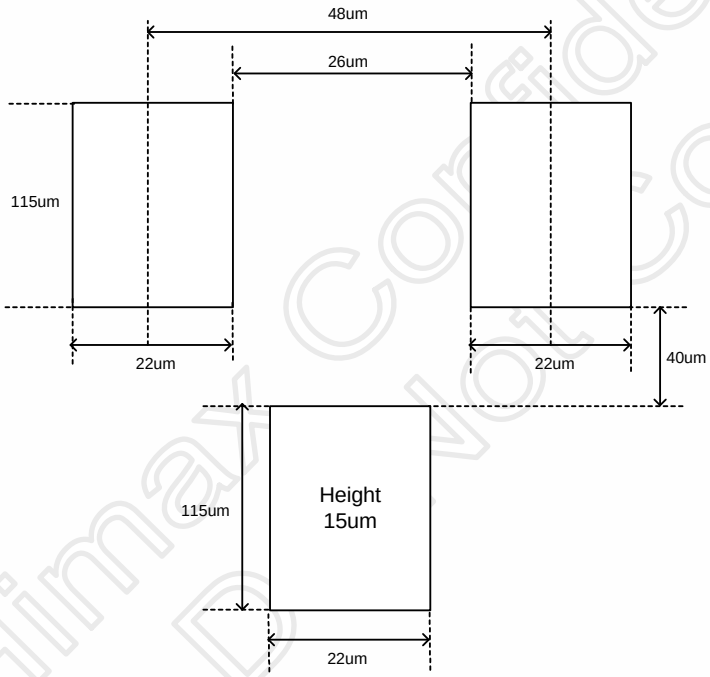


Bump size

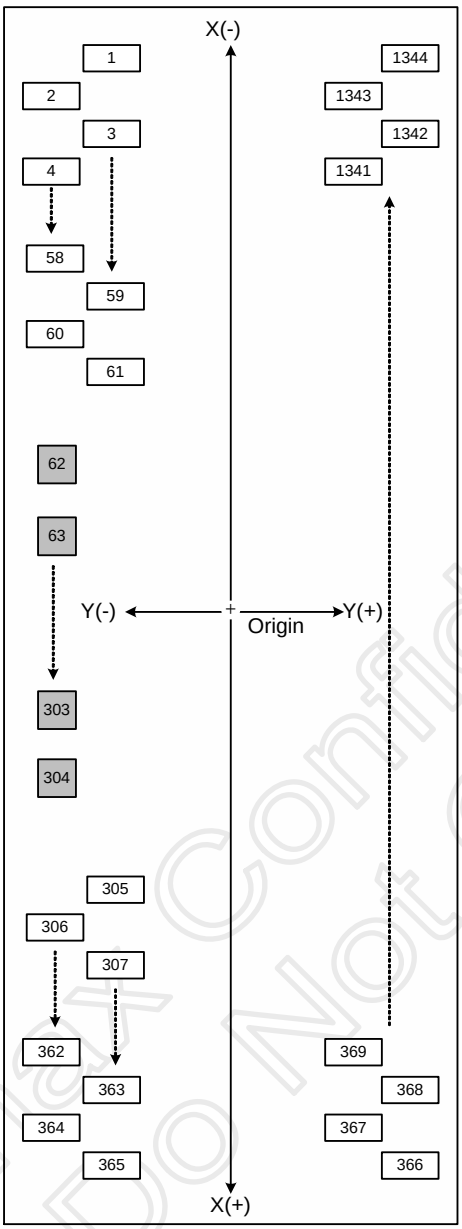
Input Bump size (type A) (pad 62~pad 304)



Output Bump size (type B) (pad 1 ~ pad 61; pad 305 ~ pad 1344)



Pad Coordinate



2. Interface

The HX8312-A has a system interface circuit for data / command transferring, and a RGB interface circuit for data transferring during animated display. The system interface circuit uses data bus pins (DB17-0) defined as (R5-0, G5-0, B5-0) bits. Since the data bus pins (DB17-0) can be used as input in RGB interface circuit, the HX8312-A shows animated display with less wiring. Table 2. 1 shows the bus pin used in every interface circuit with different external setting pin setting.

When HX8312-A is set up for unique interface mode, the input data bus pins which are not used must be fixed at IOVCC or VSSD.

External Setting Pin				Interface Mode	
NWRGB	PSX	RS	VSYNC, HSYNC , DENA , DOTCLK	Command transfer	Display Data Transfer
0	0	0	Fixed	System Interface Circuit (Parallel Bus)	-
0	0	1	Fixed	-	System Interface Circuit (Parallel Bus)
0	1	0	Fixed	System Interface Circuit (Serial Bus)	-
0	1	1	Fixed	-	System Interface Circuit (Serial Bus)
1	0	0	Input	System Interface Circuit (Parallel Bus)	-
1	0	1	Input	-	RGB Interface Circuit
1	1	0	Input	System Interface Circuit (Serial Bus)	RGB Interface Circuit
1	1	1	Input	-	RGB Interface Circuit

Table 2. 1 Interface Type

Note:
1. The NWRGB is the D0 bit of R02h register.
2. System interface (parallel and serial bus) circuit is not available when external pin RGB_nCPU = "1". All operation from system interface input are not available.
3. Please make sure that RGB interface circuit is only used for display data RAM accessed, and can not be used for register accessed.

2.1 System Interface Circuit

The system interface circuit in HX8312-A supports 18-/16-/8-bit bus width parallel bus system interface for I80 series and M68 series CPU, and 18-/16-bit serial bus system interface for serial data input. When NCS = "L" and RGB_nCPU = "L", the parallel and serial bus system interface of the HX8312-A become active and data transfer through the interface circuit is available. The RS pin specifies whether the system interface circuit access is to the register command or to the display data RAM. The input bus format of system interface circuit is selected by external pins setting. For selecting the input bus format, please refer to Table 2. 2, 2. 3.

C86	Input signal format selection
0	Format for I80 series MPU
1	Format for M68 series MPU

Table 2. 2 MPU selection

Interface Type	External Setting Pin					Bus Width	Bit number in a pixel	Transferring Method of RAM data	Transferring Method of Command
	PSX	BWS1	BWS0	DTX2	DTX1				
MPU1	0	0	0	x	x	18-bit parallel	18-bits	18-bit collective	16-bit collective
MPU2	0	1	0	0	1	16-bit parallel	18-bits	9-bit twice	
MPU3	0	1	0	1	1			16-bit + 2-bit	
MPU4	0	1	0	0	0		16-bits	16-bit collective	
MPU5	0	1	1	0	1	8-bit parallel	18-bits	6-bit 3 times	8-bit twice
MPU6	0	1	1	1	1			8-bit+8-bit+2-bit	
MPU7	0	1	1	1	0		16-bits	8-bit twice	
MPU8	1	0	1	x	x	18-bit serial	18-bits	18-bit serial	18-bit serial
MPU9	1	1	1	x	x	16-bit serial	16-bits	16-bit serial	16-bit serial

Table 2. 3 Input bus format selection of system interface circuit

2.1.1 Parallel Bus System Interface

The input / output data from data pins (DB17-0) and signal operation of the I80/M68 series parallel bus interface as listed in Table 2. 4 and Table 2. 5.

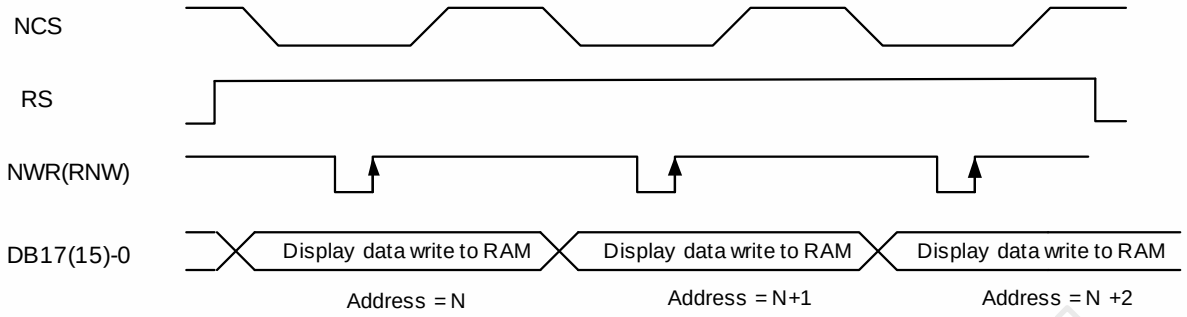
Operations	NWR(RNW)	NRD(E)	RS
Write command to register	0	1	0
Read command from register	1	0	0
Write display data to RAM	0	1	1
Read display data from RAM	1	0	1

Table 2. 4 Data pin function for I80 series CPU

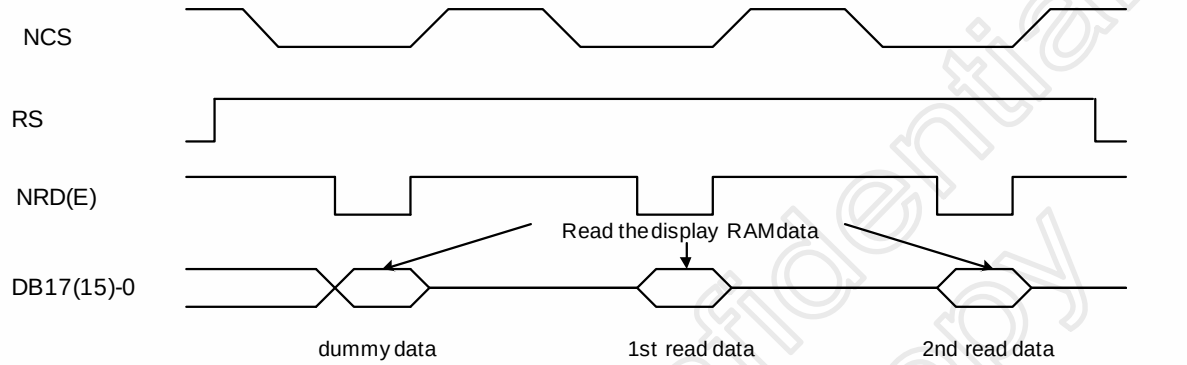
Operations	NWR(RNW)	NRD(E)	RS
Write command to register	0	1	0
Read command from register	1	1	0
Write display data to RAM	0	1	1
Read display data from RAM	1	1	1

Table 2. 5 Data pin function for M68 series CPU

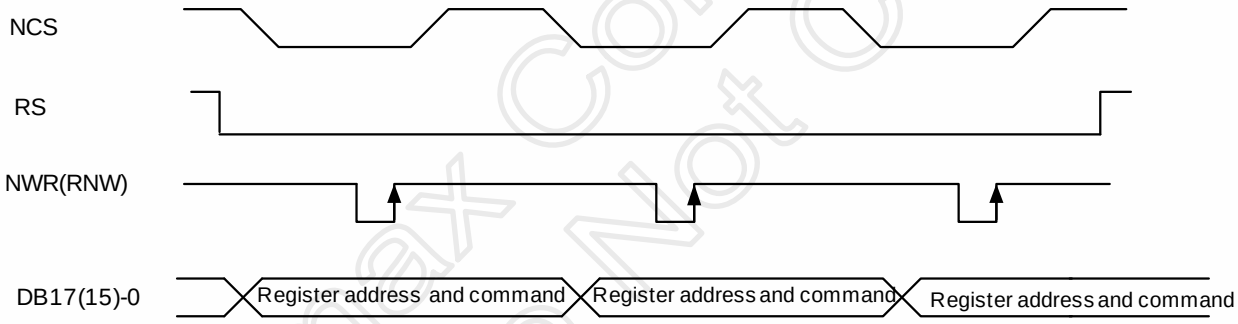
Write to the display data RAM (MPU1 , MPU4)



Read the display data RAM (MPU1 , MPU4)



Write to the register (MPU1~ MPU4)



Read the register (MPU1~MPU4)

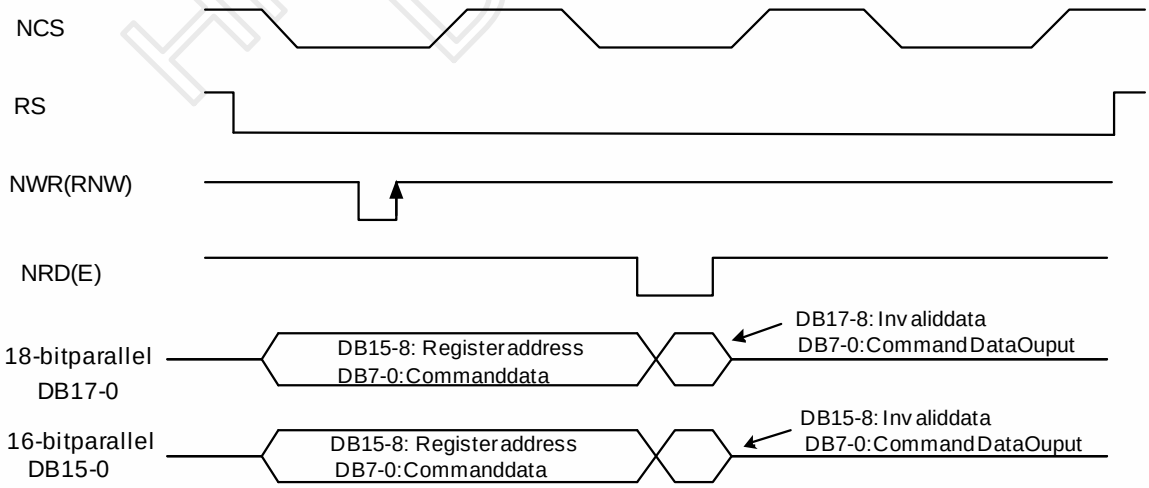
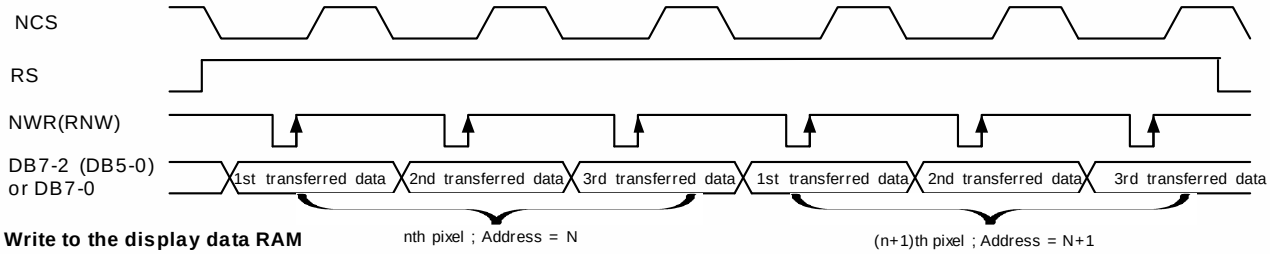


Figure 2. 1 18 / 16-bit Bus Width Parallel Bus Interface Timing (for I80 series MPU)

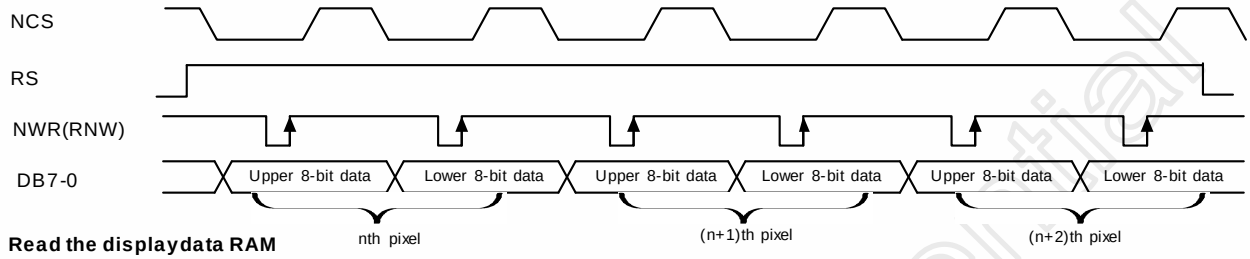
Write to the display data RAM

18-bit display data (6-bit x 3 transfers / 8-bit + 8-bit + 2-bit transfers)



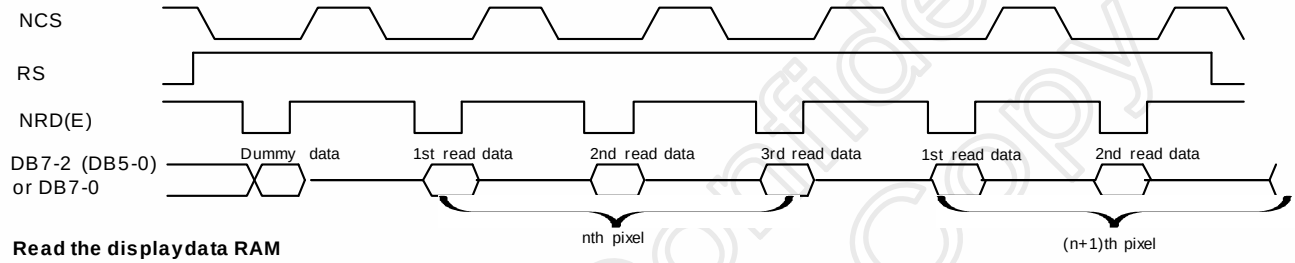
Write to the display data RAM

16-bit display data (8-bit x 2 transfers)



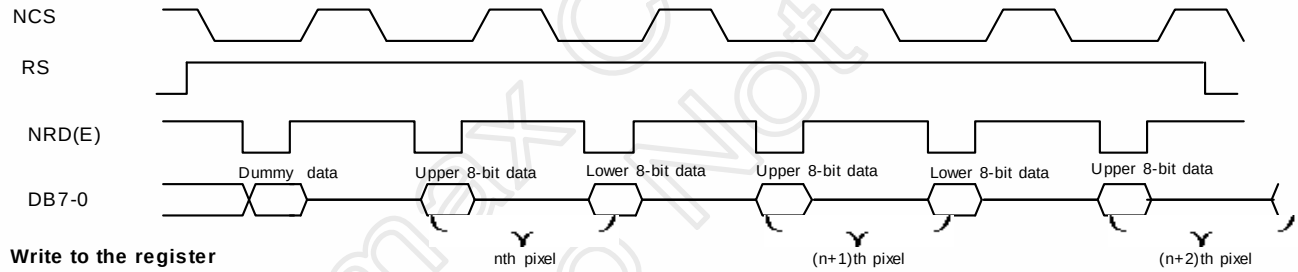
Read the displaydata RAM

18-bit display data (6-bit x 3 transfers / 8-bit + 8-bit + 2-bit transfers)

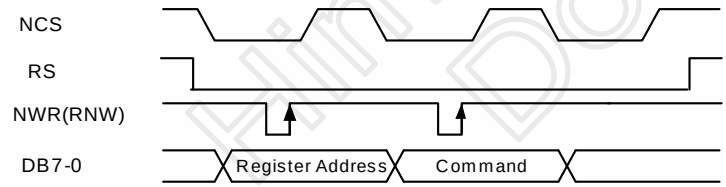


Read the displaydata RAM

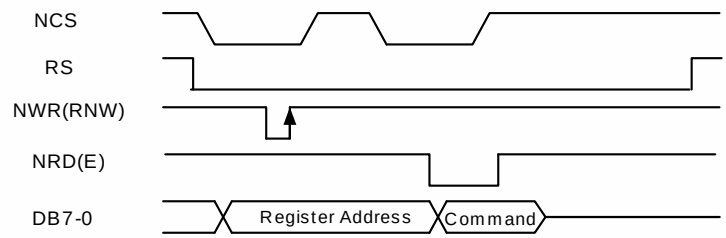
16-bit display data (8-bit x 2 transfers)



Write to the register



Read the register



DB7-2 or DB5-0 selection in 6-bit x 3 input mode is decided by MSBF (D0 bit) of R157

Figure 2. 2 8-bit Bus Width Parallel Bus Interface Timing (for I80 series MPU)

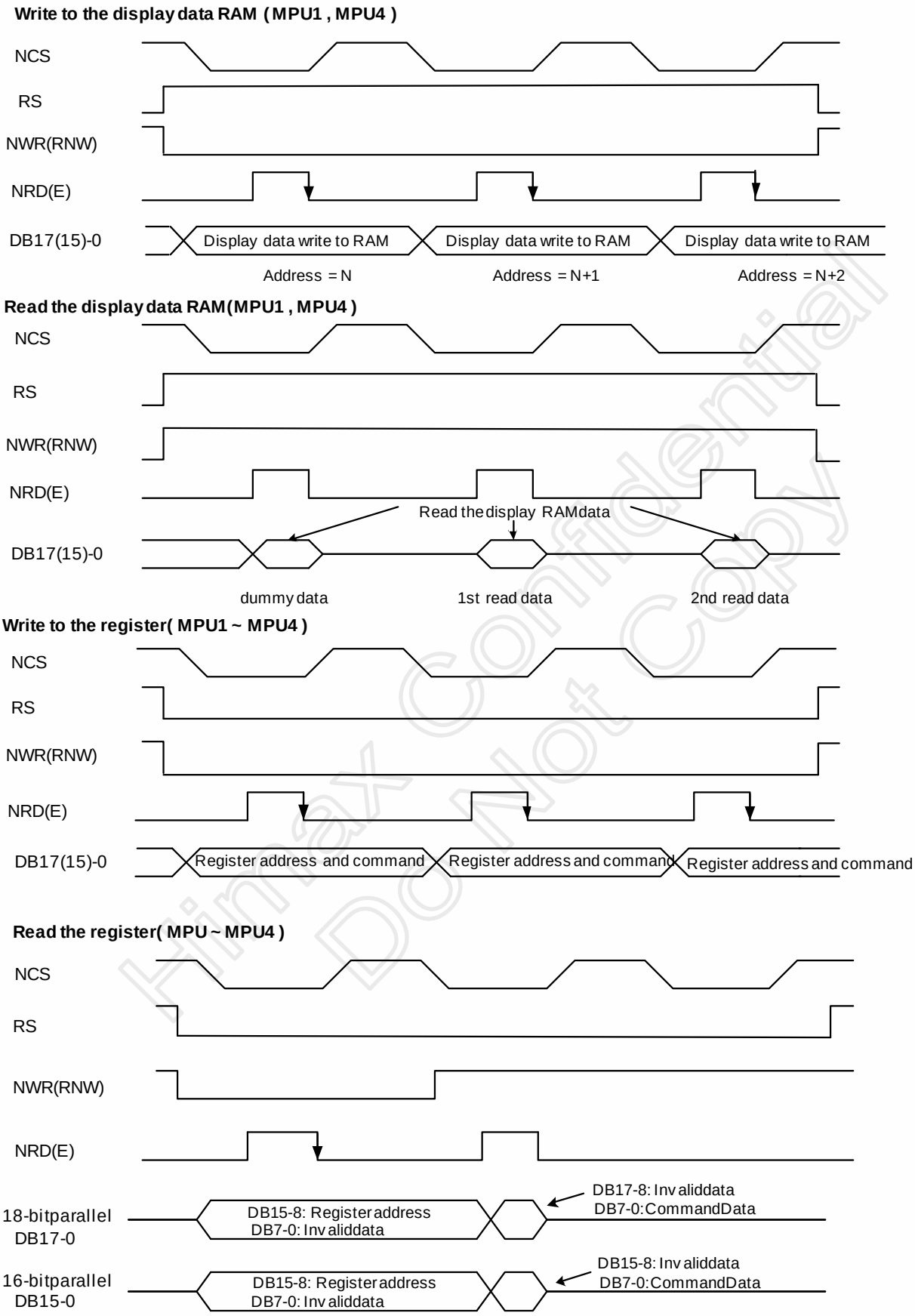


Figure 2. 3 18 / 16-bit Bus Width Parallel Bus Interface Timing (for M68 series MPU)

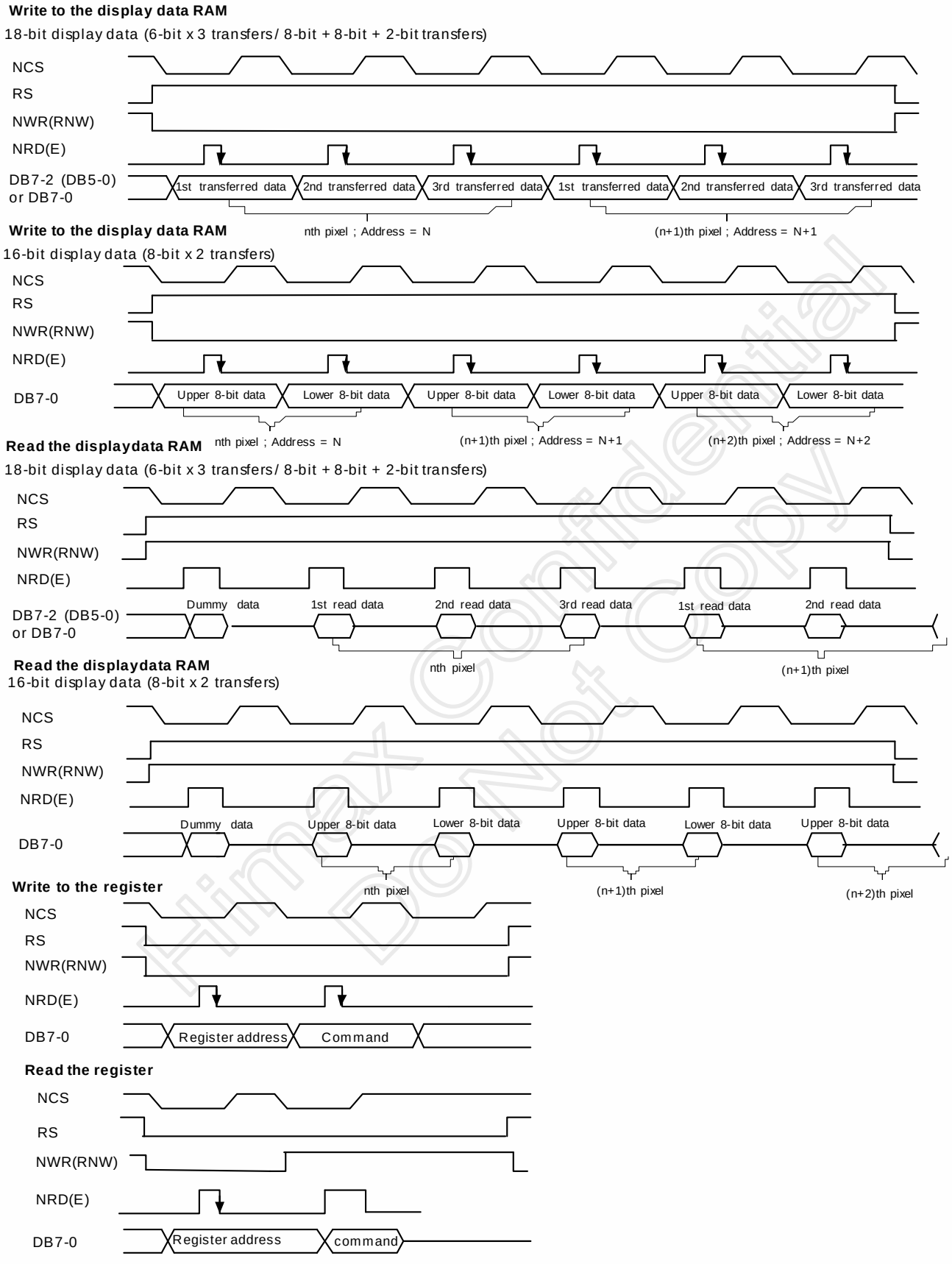


Figure 2. 4 8-bit Bus Width Parallel Bus Interface Timing (for M68 series MPU)

2.1.2 Serial Bus System Interface

The HX8312-A supports the 18/16-bit serial bus system interface. The serial bus interface mode is enabled through the chip select input (NCS), and accessed via a three-wire control pin consisting of the serial input data (SDI), serial output data (SDO), and the serial transfer clock (SCL). The selection of read / write operation is made by NWR(RNW) pin, and the RS pin specifies whether the access is to the register command or to the display data RAM. Please remember to complete one data transfer operation by the 16-clock SCLK input when the 16-bit serial interface is in use, and by the 18-clock SCLK input when 18-bit serial interface is in use.

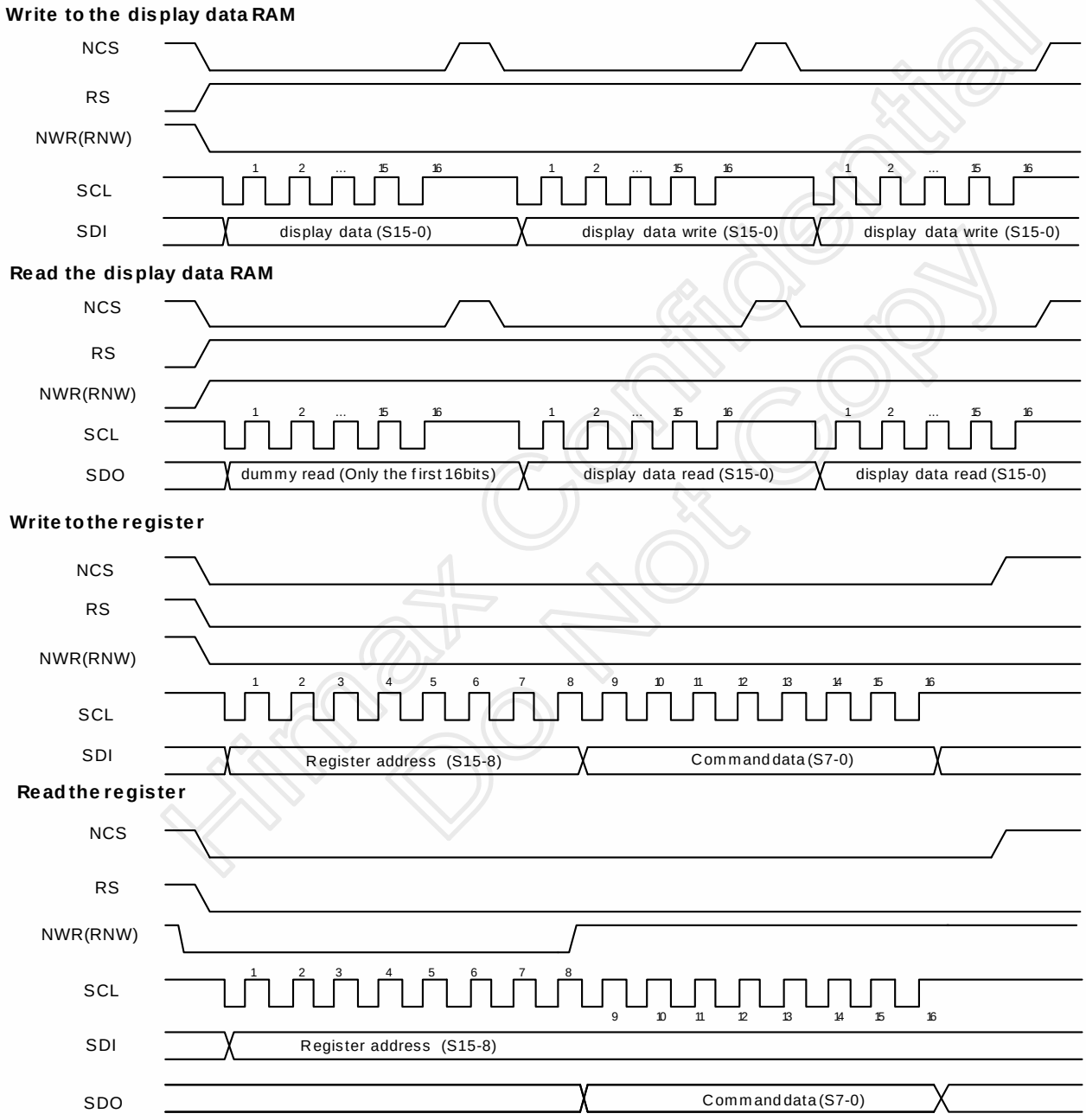
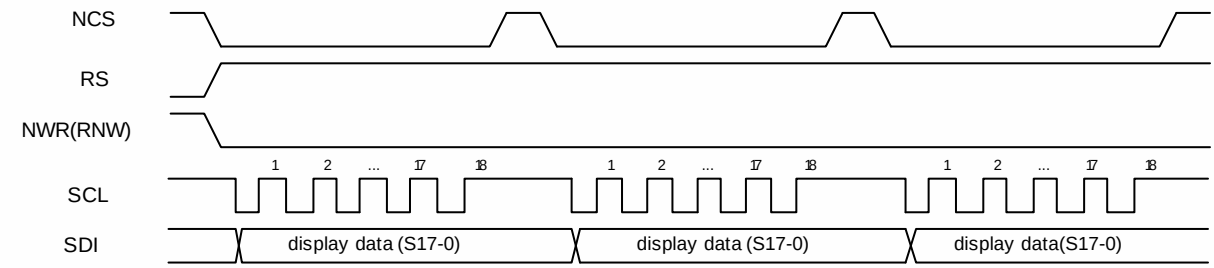
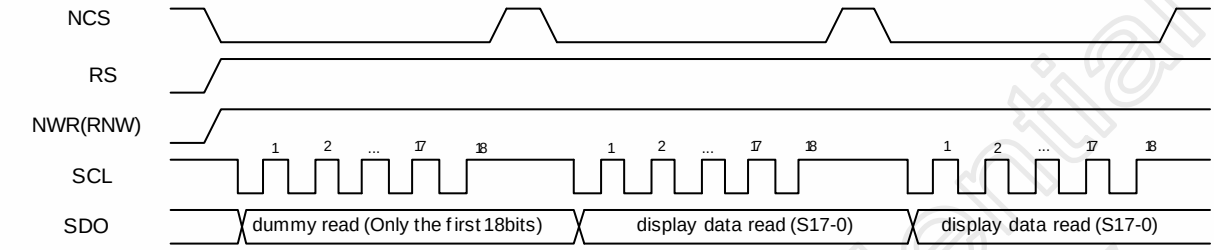


Figure 2. 5 16–bit Serial Bus Interface Timing (SCLEG1=SCLEG2=0)

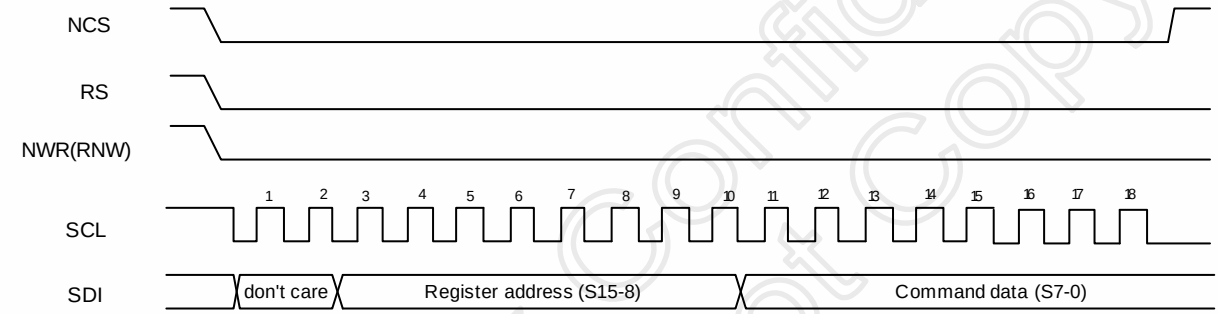
Write to the display data RAM



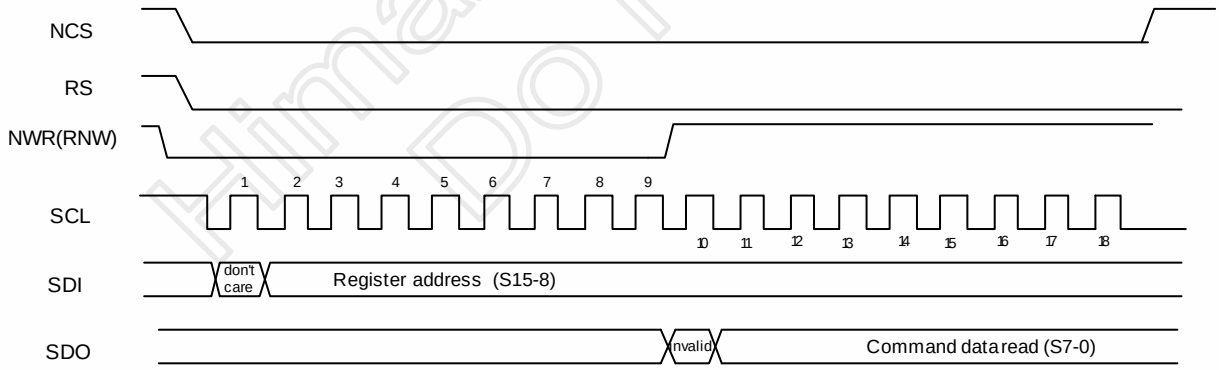
Read the displaydata RAM



Write to the registers



Read the registers



After sending a command and display data in an 18-bit unit, set nCS as "H", and then send the next command and display data.

Figure 2. 6 18–bit Serial Bus Interface Timing (SCLEG1=SCLEG2=0)

When the serial bus interface is in use, the external pins SCLEG1-0 setting determine the effective edge operation of SCLK for SDI data latch and SDO data output. Please refer to Table 2. 6 and Figure 2. 7.

SCLEG1	SCLEG0	Active level of SCLK	Latch Timing of SDI	Output Timing of SDO
0	0	Low Level	Rising edge of SCLK	Falling edge of SCLK
0	1	Low Level	Falling edge of SCLK	Rising edge of SCLK
1	0	High Level	Falling edge of SCLK	Rising edge of SCLK
1	1	High Level	Rising edge of SCLK	Falling edge of SCLK

Table 2. 6 Relation between SCLEG1-0 setting and effective edge operation of SCLK

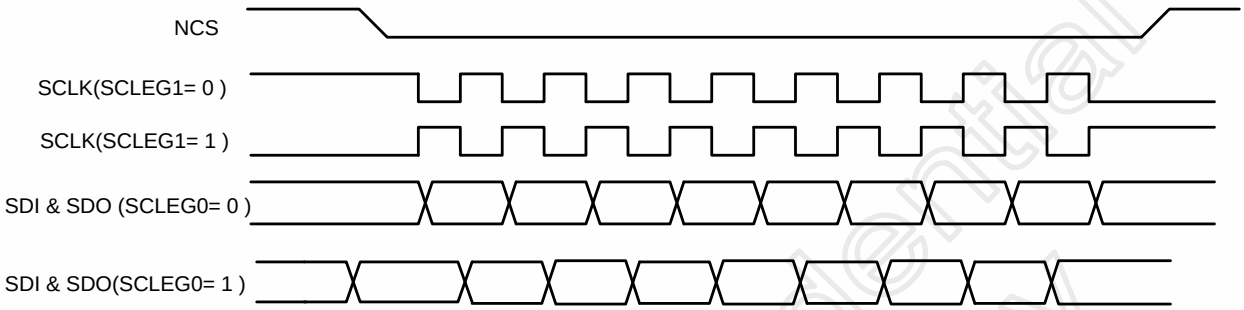


Figure 2. 7 The effective edge of SCLK with SCLEG1-0 setting

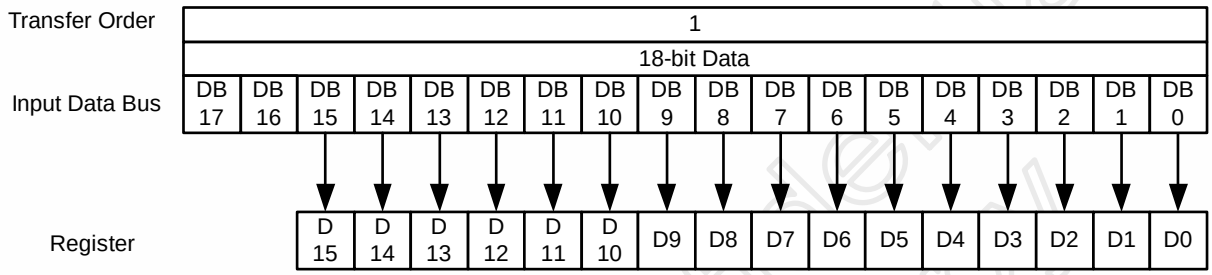
2.1.3 Relation between Register Command Data Format and Input Bus

The RS pin specifies whether the access is to the register command or to the display data RAM. The input data for register command is consist of 16 bits. The upper 8 bits (D15-8) are address and the lower 8 bits (D7-0) are data.

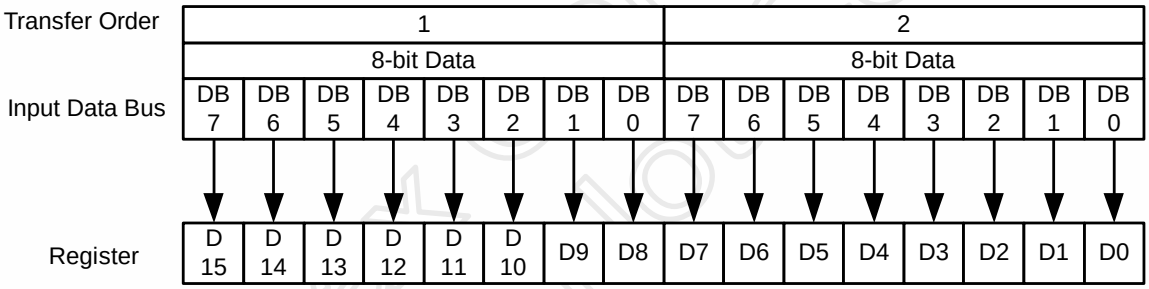
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address								Command							

The following shows the relation between register command allocation and input data bus in different MPU type input data format.

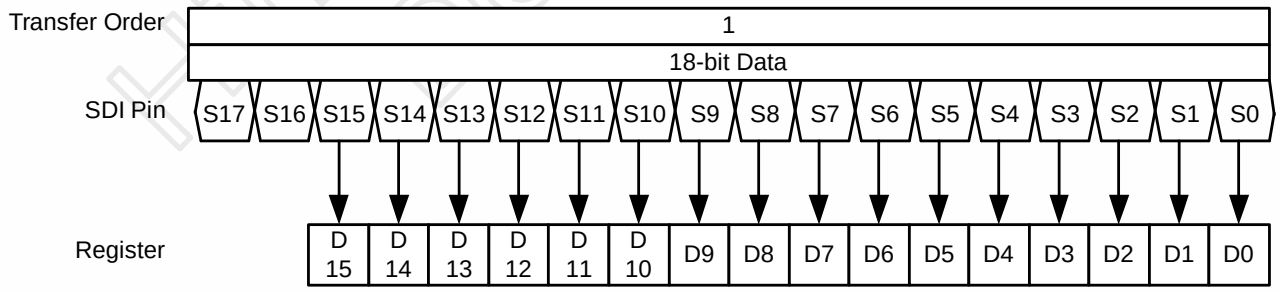
(1) MPU1, MPU2, MPU3, MPU4 Type



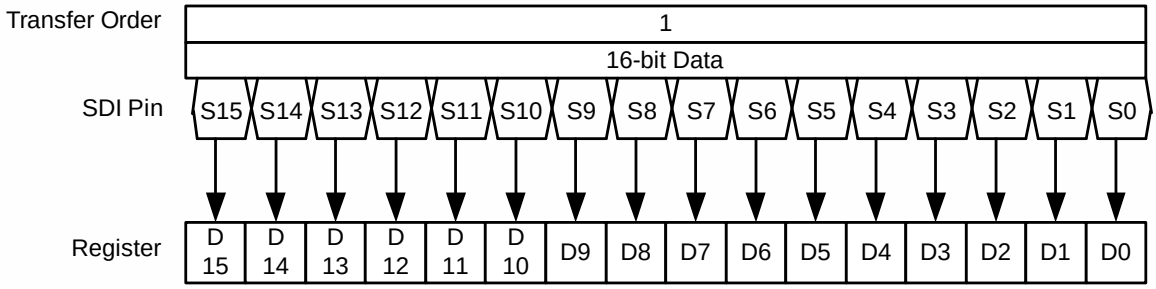
(2) MPU5, MPU6, MPU7 Type



(3) MPU8 Type



(4) MPU9 Type



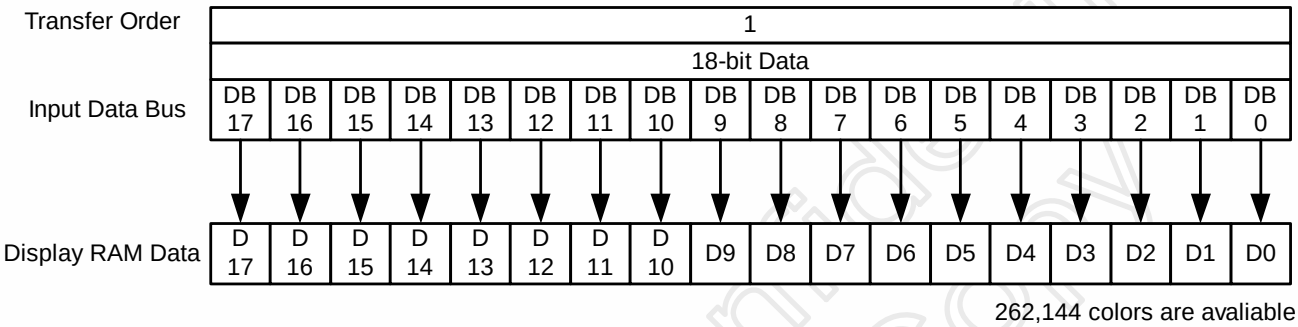
2.1.4 Relation between Display RAM Data Format and Input Bus in System Interface

The display RAM data is consist of 18 bits which include R-, G-, B-dot display level information. The (D17-12) bits are R-dot display level (D17 is MSB); (D11-6) bits are G-dot display level (D11 is MSB) ; (D5-0) bits are B-dot display level (D5 is MSB).

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

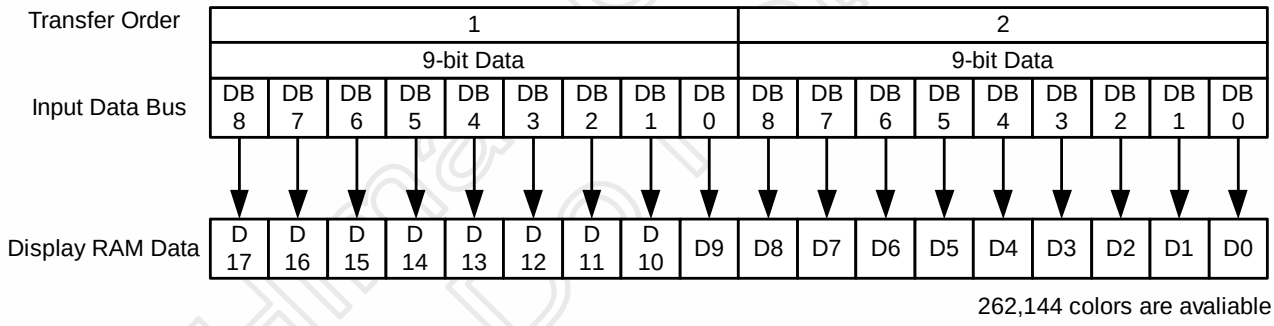
The following shows the relation between display RAM data allocation and input data bus in different MPU type input data format.

(1) MPU1 Type



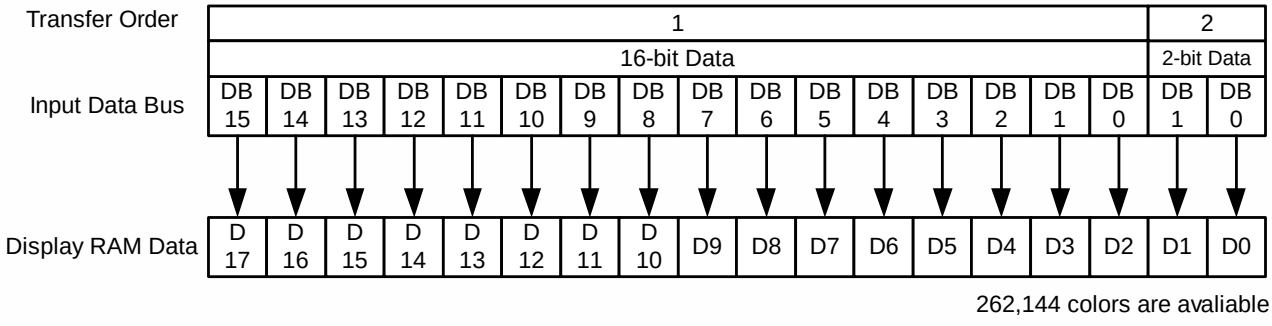
262,144 colors are avaliable

(2) MPU2 Type (9-bit ´ 2)



262,144 colors are avaliable

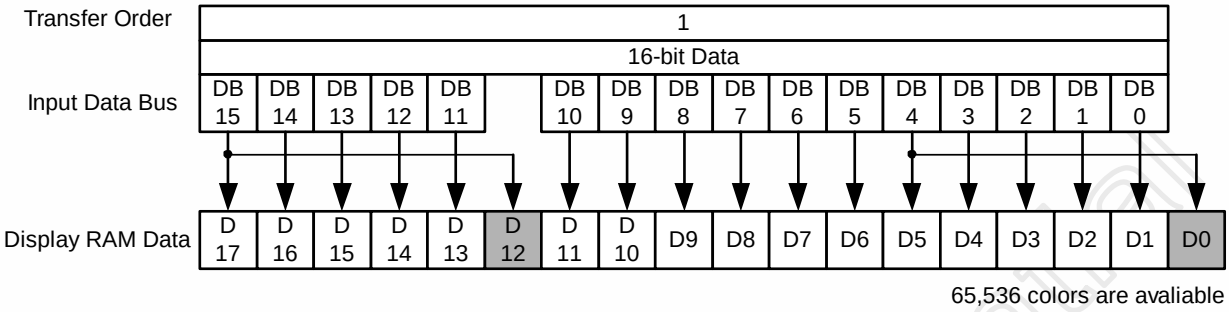
(3) MPU3 Type (16-bit + 2-bit)



262,144 colors are avaliable

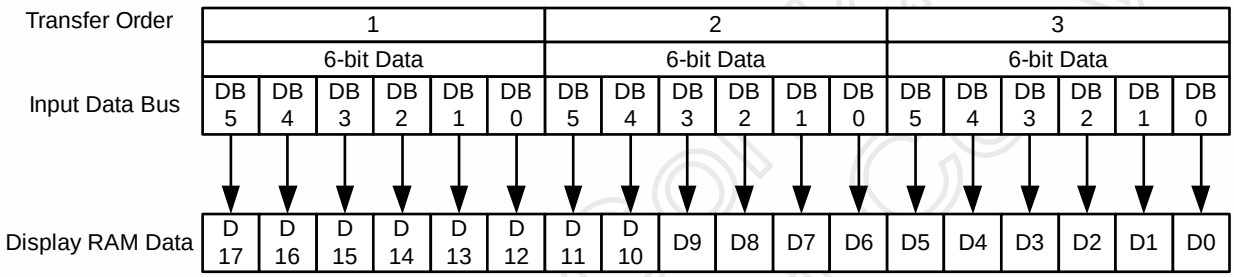
(4) MPU4 Type (16-bit × 1)

In the MPU4 type, The 16-bit data written to display RAM is expanded to 18-bit bus data automatically in the LSI. D12 of the display data RAM is compensated by the data from DB15 and D0 of the display data RAM is compensated by the data from DB4 in the transfer.



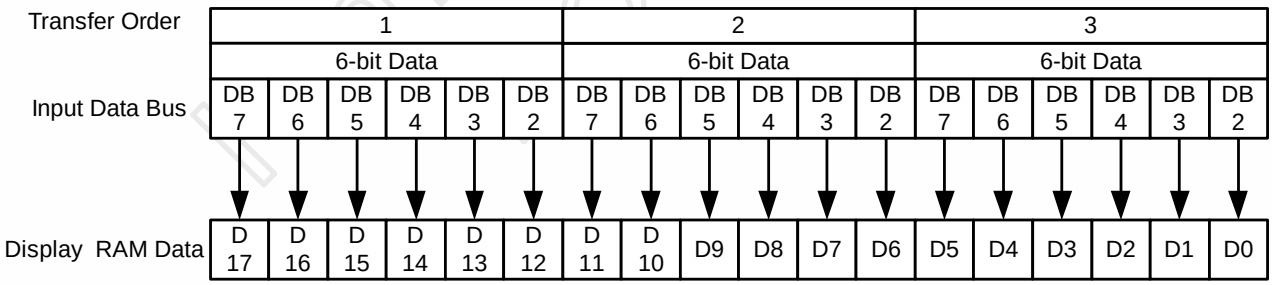
65,536 colors are avaliable

(5-1) MPU5 Type A (6-bit × 3) with (MSBF = 0 ; D0 bit of R157)



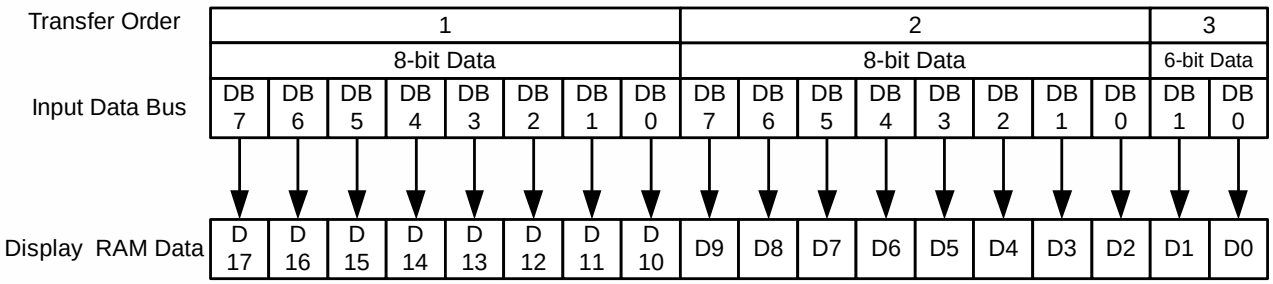
262,144 colors are avaliable

(5-2)MPU5 Type B (6-bit × 3) with (MSBF = 1; D0 bit of R157)



262,144 colors are avaliable

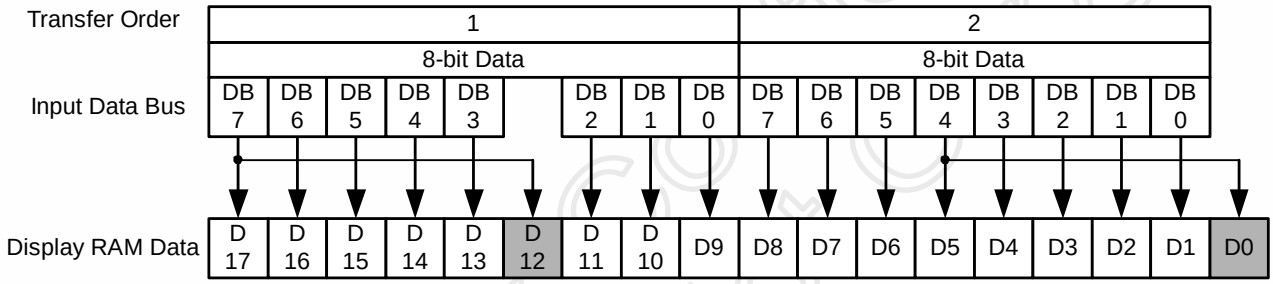
(6) MPU6 Type (8-bit + 8-bit + 2-bit)



262,144 colors are avaliable

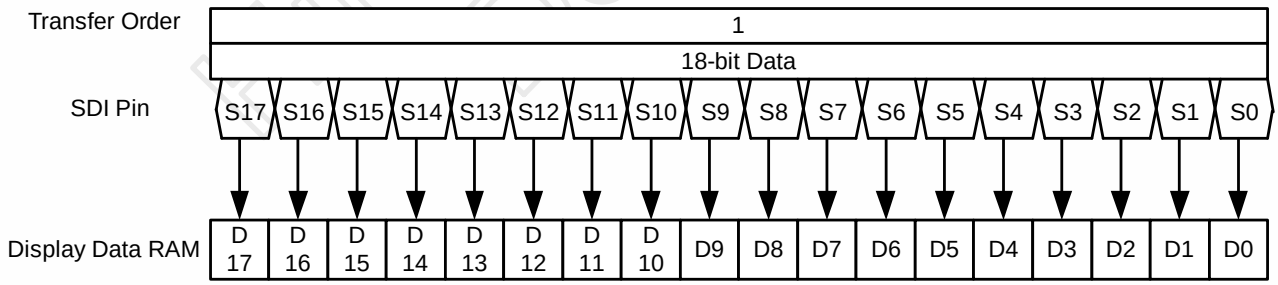
(7) MPU7 Type (8-bit ´ 2)

In the MPU7 type, The 16-bit data written to display RAM is expanded to 18-bit bus data automatically in the LSI. D12 of the display data RAM is compensated by the data from DB7 in the first transfer and D0 of the display data RAM is compensated by the data from DB4 in the second transfer.



65,536 colors are avaliable

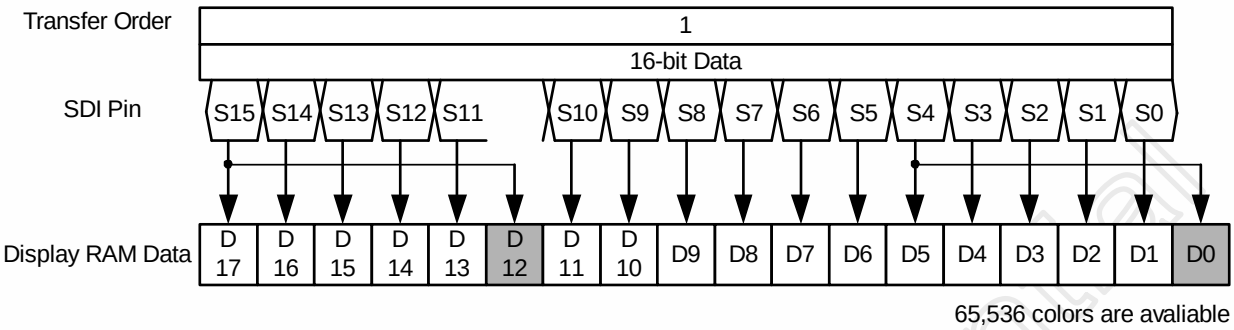
(8)MPU8 Type (18-bit serial)



262,144 colors are avaliable

(9) MPU9 Type (16-bit serial)

In the MPU9 type, The 16-bit data written to display RAM is expanded to 18-bit bus data automatically in the LSI. D12 of the display data RAM is compensated by the data from S15 and D0 of the display data RAM is compensated by the data from S4 in the transfer.



65,536 colors are avaliable

2.2 RGB Interface Circuit

The HX8312-A has the RGB interface circuit for animated display data written. RGB25-20, RGB15-10, RGB05-00 input pins are used for RGB interface circuit via data pins (DB17-0). When using the RGB interface circuit to update display RAM, please make sure to set NWRGB (D0 bit of R2) as “1”. Please make sure that register of LSI can not be accessed via RGB interface circuit.

When the data pins (DB17-0) are used for the RGB interface circuit, the bit allocation is as below.

Data Pins	RGB Pins
DB17-12	RGB25-20
DB11-6	RGB15-10
DB5-0	RGB05-00

Table 2. 7 Bit allocation when DB17-0 used for RGB interface circuit

The input bus format of RGB interface circuit is selected by external pin BWS2 and MSBF (D0 bit of R157) setting. For selecting the input bus format, please refer to Table 2. 8.

Interface Type	External Pin	Register	Interface Mode	Number of data per pixel	Transferring method of one pixel data
	BWS2	MSBF (D0 : R157)			
RGB1	0	0	18-bit	18 bits	18-bit collective
RGB2	1	0	16-bit	16 bits	16-bit collective
RGB3	0 or 1	1	6-bit	18 bits	6-bit x 3

Table 2. 8 RGB Interface Mode Selection

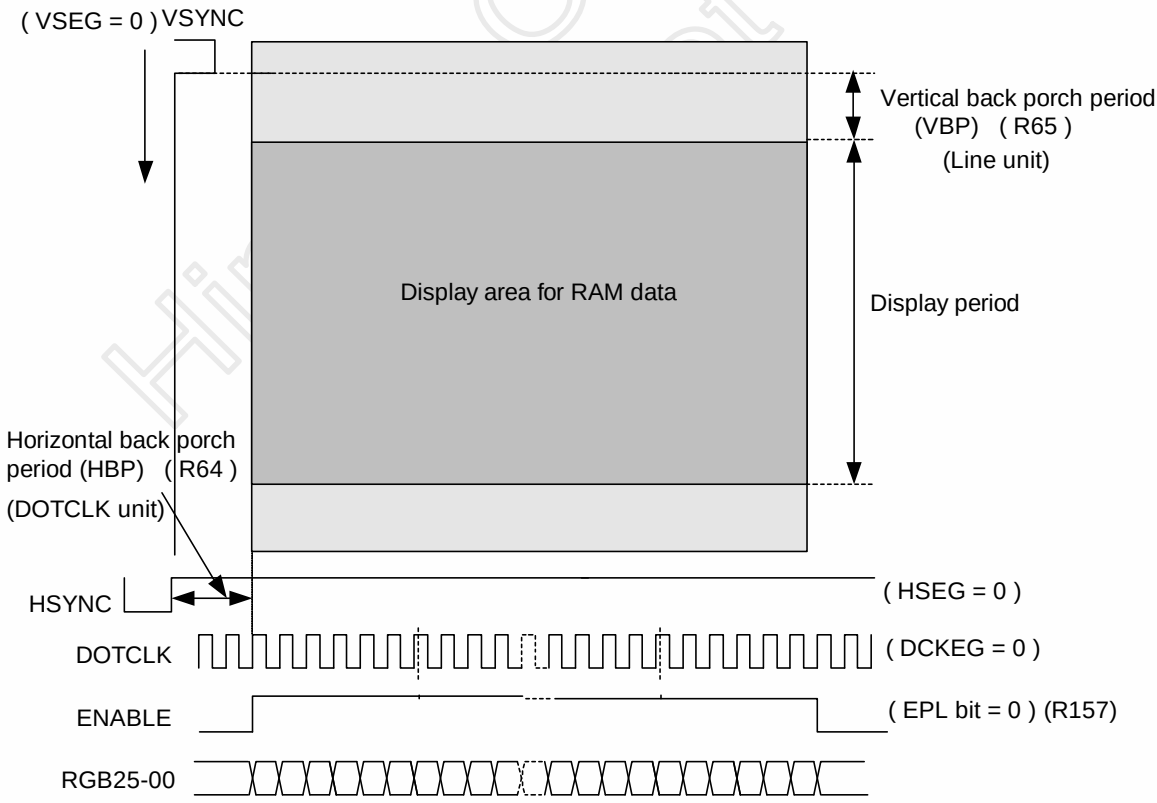


Figure 2. 8 RGB Interface Circuit Input Timing

Figure 2.9 shows the input timings of the RGB3 type input format.

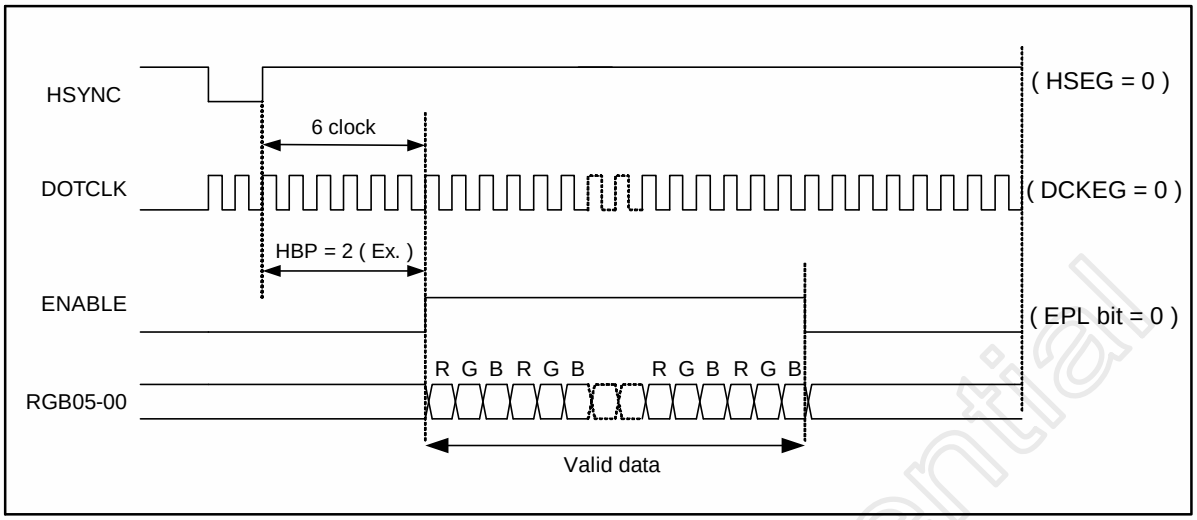
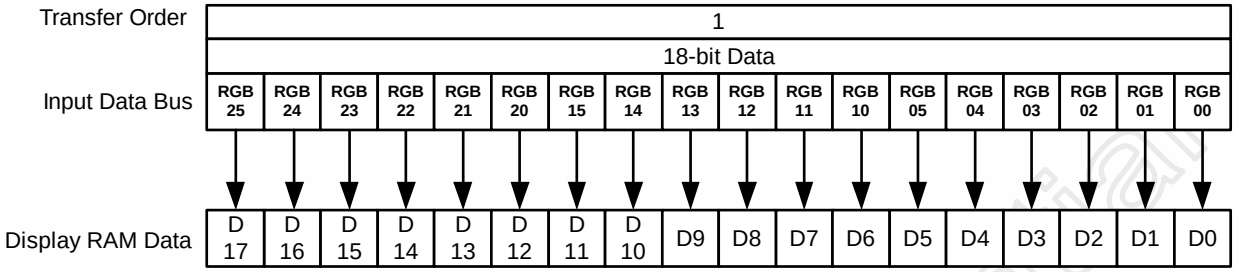


Figure 2. 9 RGB3 Type (6-bit Interface Mode) Input Timing

2.2.1 Relation between Display RAM Data Format and Input Bus

The following shows the relation between display RAM data allocation and input data bus in different RGB type input data format.

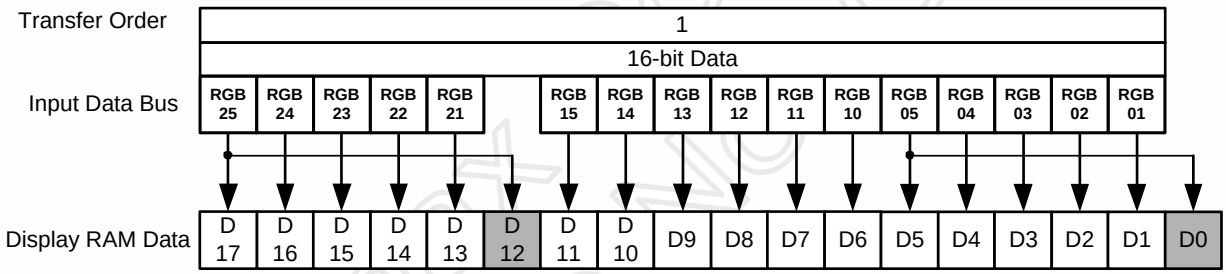
(1)RGB1 Type



262,144 colors are avaliable

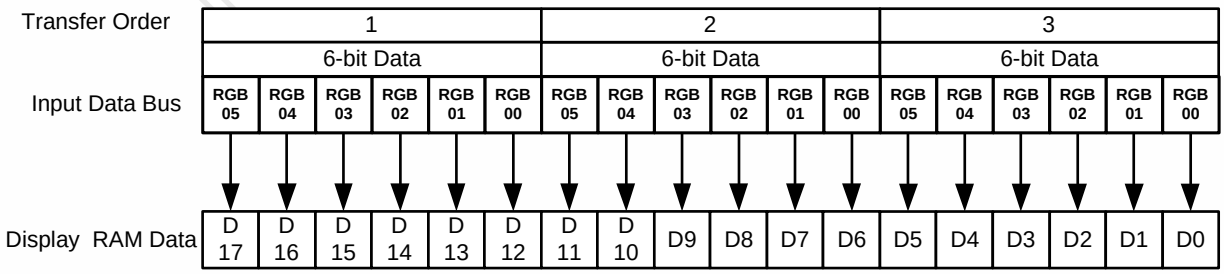
(2)RGB2 Type

In the RGB2 type, The 16-bit data written to display RAM is expanded to 18-bit bus data automatically in the LSI. D12 of the display data RAM is compensated by the data from RGB23 and RGB04 of the display data RAM is compensated by the data from DB4 in the transfer.



65,536 colors are avaliable

(3)RGB3 Type



262,144 colors are avaliable

3. Input and Synchronized Display Modes

The HX8312-A has three writing mode for display data input. Three writing modes are as follow :

(1)Through Mode: In through mode, input display data via RGB interface circuit is not written to display RAM and is displayed directly.
(2)Capture Mode: In capture mode, display data is written to display RAM via RGB interface circuit and displayed.
(3)Override Mode: In override mode, RGB pins are not available, and input display data via system interface circuit is written to display RAM and display.

Also, the HX8312-A has three synchronized display modes as listed below :

(1)Internally Synchronized Display Mode:
Display operation is synchronized with SYSCLK generated by internal oscillator.
(2)Externally Synchronized Display Mode:
Display operation is synchronized with external VSYNC, HSYNC, DOTCLK signal input.
(3)VSYNC Interface Display Mode:
Display operation is synchronized with SYSCLK and external VSYNC signal input.

Table 3. 1 shows the combinations of these modes. One out of these six modes is available by setting D4, D2, D1, D0 bits of the RGB interface register (R2). See the sections (3.1 - 3.3) for more details. When a mode is changed to another mode, HX8312-A can display correct pictures after finishing displaying the present frame.

Register R2				RGB Mode	Used Interface Circuit	Signal used to display RAM write	Display Operation	
D4	D2	D1	D0				Mode Name	Signal used to display
VMODE	RGBS	DISPCLK	NWRGB					
0	1	1	1	Through Mode	RGB Interface Circuit	No write operation	Externally Synchronized Display mode	VSYNC, HSYNC, DOTCLK
0	0	1	1	Capture Mode	RGB Interface Circuit	VSYNC, HSYNC, DOTCLK	Externally Synchronized Display mode	VSYNC, HSYNC, DOTCLK
0	X	0	1	Capture Mode	RGB Interface Circuit	VSYNC, HSYNC, DOTCLK	Internally Synchronized Display mode	SYSCLK (*1)
0	X	0	0	Override Mode	System Interface Circuit	NCS, NRD(E), NWR(RNW) (*3)	Internally Synchronized Display mode	SYSCLK (*1)
0	X	1	0	Override Mode	System Interface Circuit	NCS, NRD(E), NWR(RNW) (*2)	Externally Synchronized Display mode	VSYNC, HSYNC, DOTCLK
1	0	0	0	-	System Interface Circuit	NCS, NRD(E), NWR(RNW) (*2)	VSYNC interface mode	VSYNC, SYSCLK

Table 3. 1 Display Mode Set up

Note:1: SYSCLK: system clock signal generated by internal oscillator.
2: Serial bus interface pins are also available.
3: X ="1" or "0" (optional)

3.1 The Operation of Each Mode

3.1.1 Externally synchronized display mode + through mode

As Table 3. 1 shows, the HX8312-A enters "externally synchronized mode + through mode" by setting D4, D2, D1 and D0 bits of the RGB interface register (R2) as "0111". In this mode, display data is displayed in synchronization with VSYNC, HSYNC and DOTCLK , and the display data of display area defined by RGB start register 1 (R60), RGB start register 2 (R61), RGB end register 1 (R62) and RGB end register 2 (R63), is inputted via RGB interface circuit without being written to the display RAM and display directly. The display data in the display RAM outside the display area defined by R60-R63 is not updated in this mode so the same display data is displayed. NWRGB(D0 bit of R2) must be set to “0” when it is necessary to update display RAM data outside the display area defined by R60-R63, and then display data must be inputted via system interface pins.

In this mode, the vertical back porch register VBP4-0 (D4-0 of R65) needs to be set the value the same as vertical back porch of input signal. The horizontal back porch register HBP4-0 (D4-0 of R64) needs to be set the value the same as (horizontal back porch-2) of input signal. See Figure 3. 1.

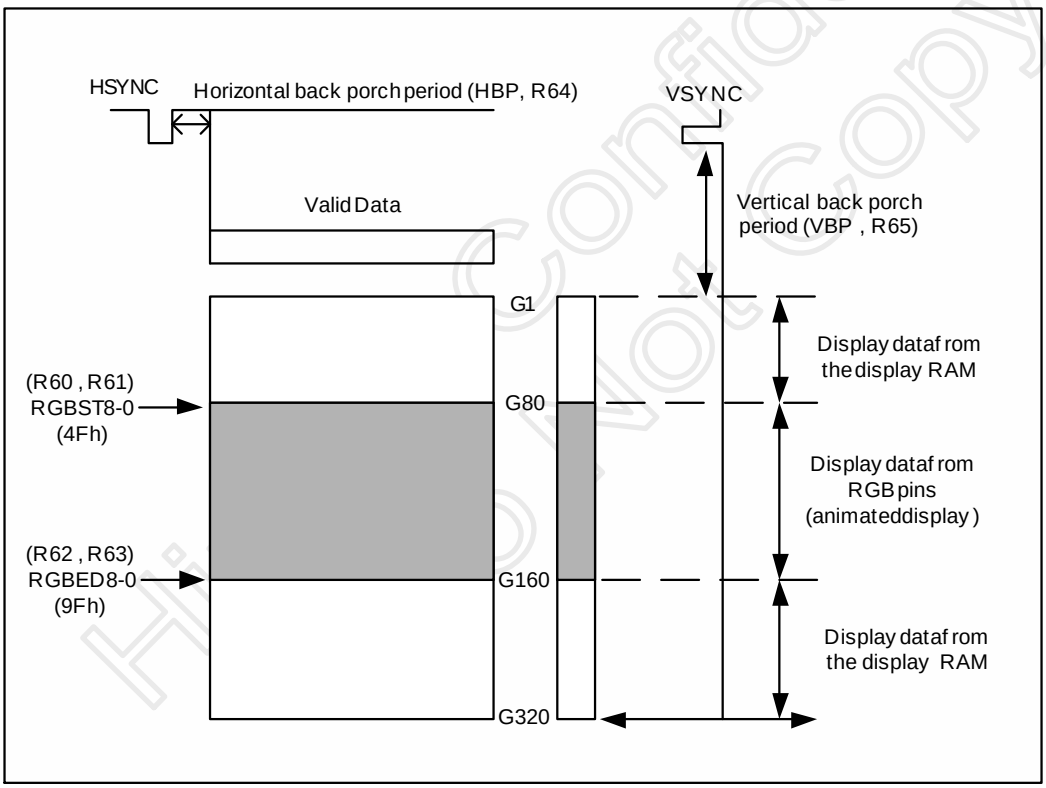


Figure 3. 1 Display example in the externally synchronized display mode + through mode

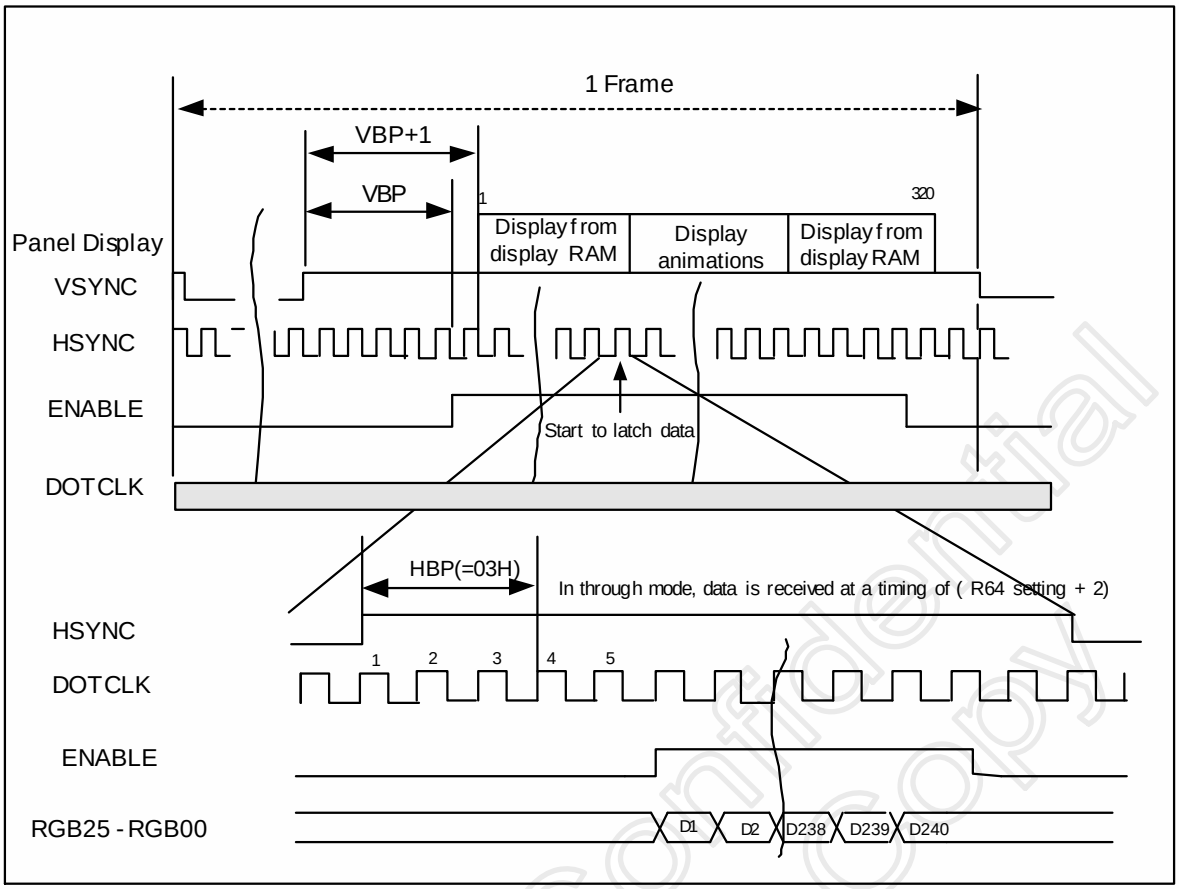


Figure 3. 2 Display and Input Timing of the externally synchronized display mode + through Mode (VSEG ="0", HSEG = "0", DCKEG = "0", EPL = "0")

3.1.2 Externally synchronized display mode + capture mode

As Table 3. 1 shows, by setting D4, D2, D1 and D0 bits of the RGB interface register (R2) as "0011", the HX8312-A enters "externally synchronized mode + capture mode". In this mode, display data is written to the display RAM via RGB interface first and then displayed in synchronization with VSYNC, HSYNC and DOTCLK by reading the display data from the display RAM in the same frame. As in Figure 3. 3, the captured area can be determined by the window area access mode. (See the "4.3 Window Address Area Access" section.) or full screen display. The display data in the display RAM outside the display area defined by window access register is not updated in this mode so the same display data is displayed. When it is necessary to update display RAM data outside the window access area, it needs to change window access area register.

In this mode, the vertical back porch register VBP4-0 (D4-0 of R65) needs to be set the value the same as vertical back porch of input signal. The horizontal back porch register HBP4-0 (D4-0 of R64) needs to be set the value the same as horizontal back porch of input signal. See Figure 3. 3.

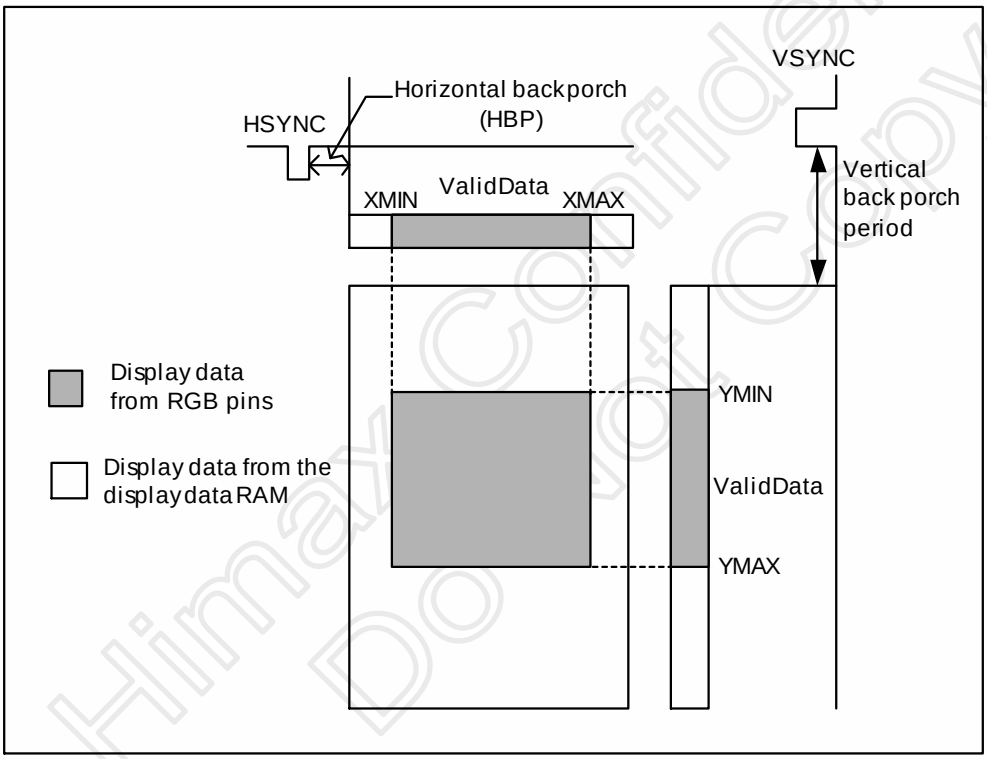


Figure 3. 3 Display example in the externally synchronized display mode + capture mode

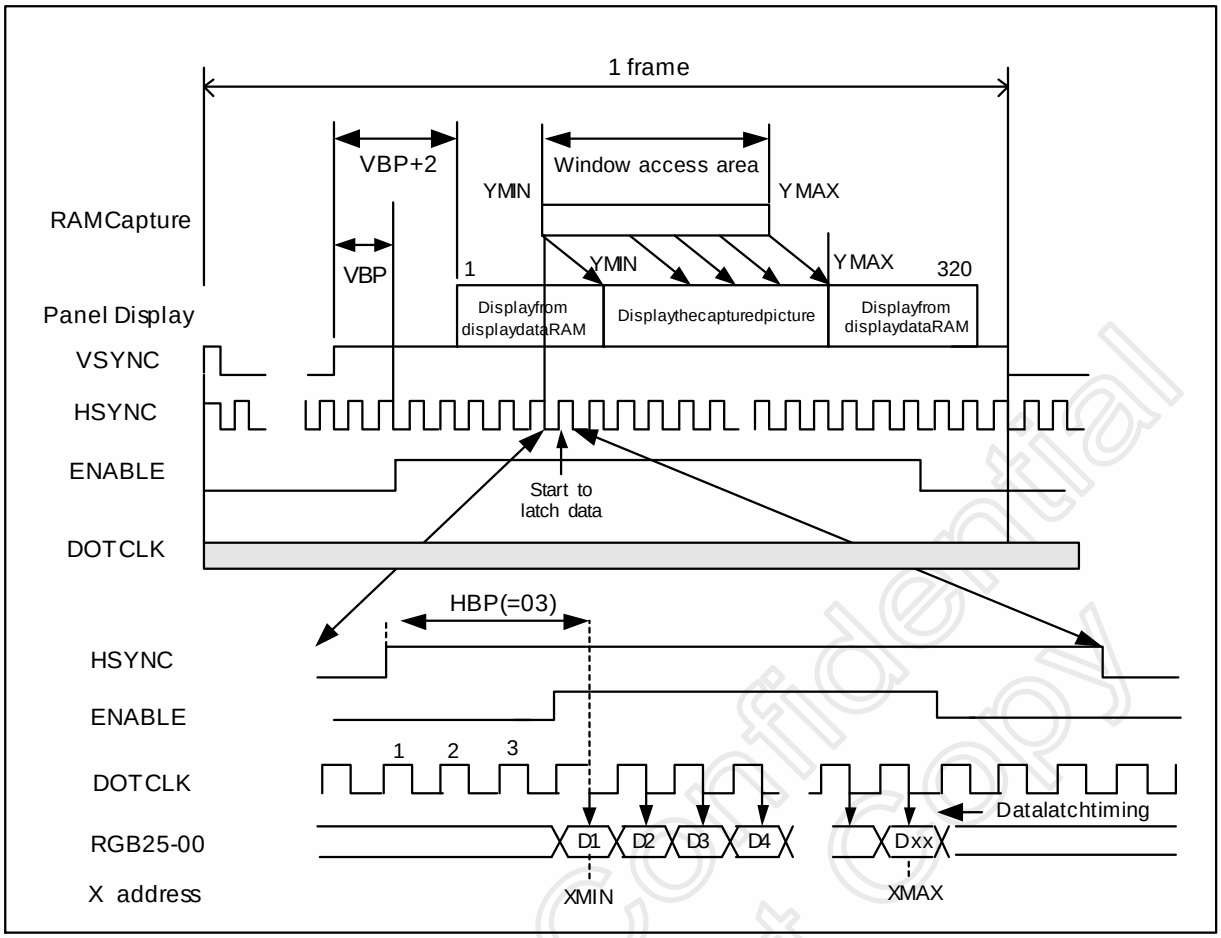


Figure 3. 4 Display and Input Timing of the externally synchronized display mode + capture mode (VSEG ="0", HSEG = "0", DCKEG = "0", EPL = "0")

3.1.3 Internally synchronized display mode + capture mode

As Table 3. 1 shows, by setting D4, D2, D1 and D0 bits of the RGB interface register (R2) as "0001", the HX8312-A enters "internally synchronized mode + capture mode". In this mode, display data is written to the display data RAM via RGB interface circuit first and then displayed in synchronization with SYSCLK (system clock signal generated by internal oscillator) by reading the display data from the display RAM to the panel. As in Figure 3. 3, the captured area are determined by the window access mode. (See the "4.3 Window Address Area Access Mode") The display data in the display RAM outside the display area defined by window access register is not updated in this mode so the same display data is displayed. When it is necessary to update display RAM data outside the window access area, it needs to change window access area register.

In this mode, 1-frame and 1-line period of display timing must be defined by internal SYSCLK instead of VSYNC and HSYNC. In this mode, the vertical back porch register VBP4-0 (D4-0 of R65) needs to be set the value the same as vertical back porch of input signal. The horizontal back porch register HBP4-0 (D4-0 of R64) needs to be set the value the same as horizontal back porch of input signal.

3.1.4 Internally synchronized display mode + override mode

As Table 3. 1 shows, by setting D4, D2, D1 and D0 bits of the RGB interface register (R2) as "0000", the HX8312-A enters "internally synchronized mode + override mode". In this mode, display data is written to the display data RAM via system interface circuit first and then displayed in synchronization with SYSCLK by reading the display data from the display RAM to panel.

In this mode, 1-frame and 1-line period of display timing must be defined by internal SYSCLK instead of VSYNC and HSYNC.

3.1.5 Externally synchronized display mode + override mode

As Table 3. 1 shows, by setting D4, D2, D1 and D0 bits of the RGB interface register (R2) as "0010", the HX8312-A enters "Externally synchronized mode + override mode". In this mode, display data is written to the display data RAM via system interface circuit first and then displayed in synchronization with VSYNC, HSYNC, DOTCLK.

In this mode, the display blanking period is determined by the settings of the horizontal back porch register (R64) and the vertical back porch register (R65).

3.2 VSYNC Interface Mode

The HX8312-A supports the VSYNC interface mode, which can display animated displays with the system interface circuit and the frame synchronization signal VSYNC.

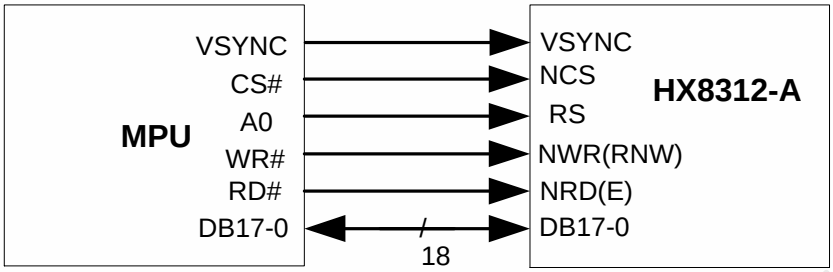


Figure 3. 5 VSYNC Interface to MPU

By setting D4 = "1" (VMODE) and D3-D0="0000" of the RGB interface register (R2), the VSYNC interface becomes available. In the VSYNC interface mode, the internal display operation is synchronized with SYSCLK, however, the frame starting of display operation is determined by VSYNC. (Therefore, VSYNC signal needs always exist.)

In the VSYNC interface mode, writing of display data to the display RAM must be performed before outputting that pixel data in the same allocation of RAM for smooth animation display. Therefore, the VSYNC interface has some constraints in the internal clock and the RAM write speed via the system interface circuit. It requires display RAM write speed more than the minimum value that system processed and displayed. The system clock (SYSCLK) in VSYNC interfaces mode can be computed by the following formula that used some parameters with VFP, VBP and display lines duration (320 line):

$$\text{SYSCLK } frequency(fs) = Frame\,Frequency \times [Display\,Lines(321) + VBP + VFP] \times HCK \times frequency\ \ fluctuation$$

VBP (Vertical Back porch) : set by R65
VFP (Vertical Front porch) : defined automatically (Min. 1 line is necessary)
HCK : The clock number of SYSCLK specifies the horizontal line period (1H), which is set by R139

The parameter of frequency fluctuation is ascribed to the external resistor or voltage variation, fabrication process condition, external temperature and humidity condition etc.

Then the minimum speed for display RAM write can be computed by the following formula:

$$The\ Min.\ RAM\ Write\ Speed\ [Hz] \geqq \frac{240(pixel)\times DisplayLines(321)\times fs}{[VBP + DisplyLines(NL) - margin\ lines]\times HCK}$$

The margin line means when operate in VSYNC interface mode, it must be remained the several lines in advance for protection between the actual line of the display operation and the line address for the RAM write data operation.

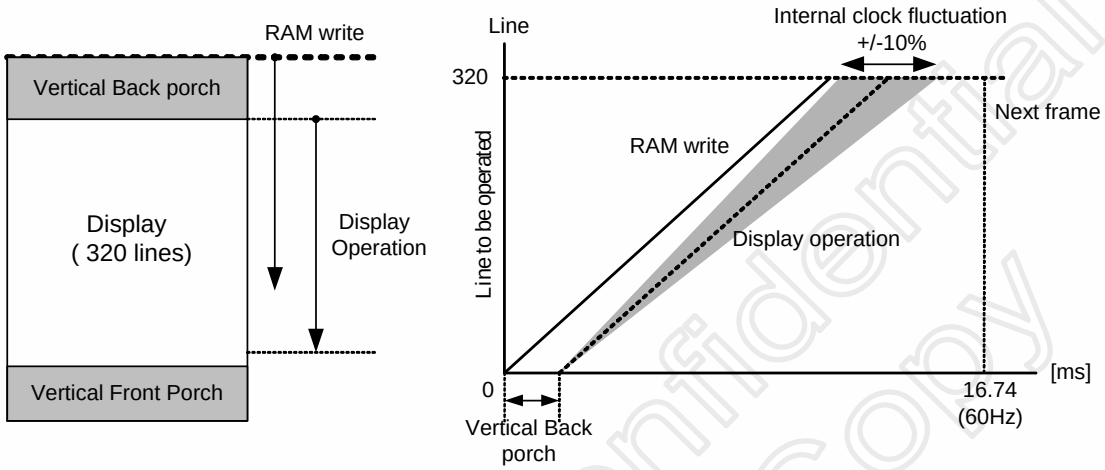


Figure 3. 6 VSYNC Interface Mode Operation

The mode transition flow between internally synchronized display mode and VSYNC interface mode is as Figure 3. 7.

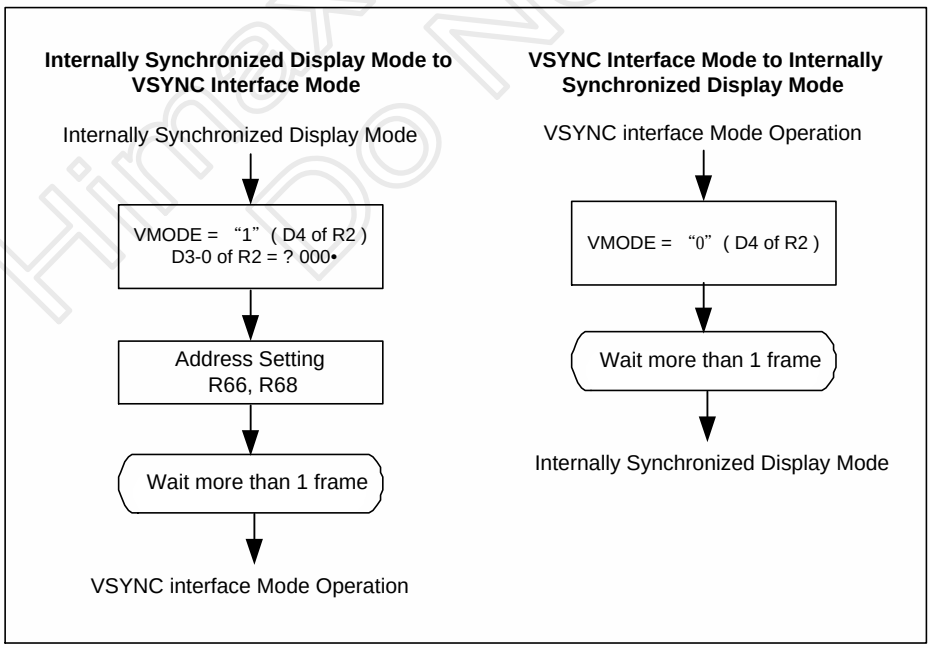


Figure 3. 7 VSYNC Interface Mode and Internally Synchronized Mode Transition

3.3 Internal Clock Mode

The clock number of SYSCLK which is stored in the line clock register (R139) is used to specify the one horizontal line period (1H) in the internally synchronized display mode. The one horizontal line period (1H) can be adjusted by two ways. One is by calibration and another is by setting the clock number of one horizontal line period (1H) in a register. The horizontal cycle adjustment mode is defined by CLKM (D0 bit of the line cycle adjustment mode register , R141). Clock numbers will be stored into line clock register (R139) in both cases. In case of calibration, the value will be stored automatically. In case of register set up ,the value will be set from MPU.

D0=CLKM	Setting Method
0	Calibration Mode
1	Register Setup Mode

Table 3. 2 Line Frequency Adjustment

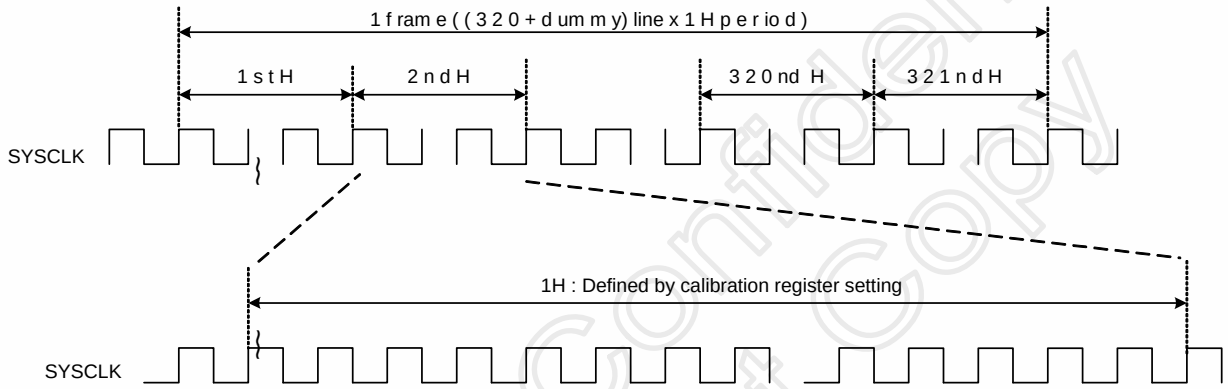


Figure 3. 8 One Line Clock Number in Internal Clock Mode

3.3.1. Adjusting the one horizontal line period (1H) by calibration

Setting OC (D0 bit of the calibration register, R45) as "0" starts calibration. The calibration starts from the first positive edge of SYSCLK after D0=OC is set as "0". The HX8312-A counts the number of positive edges of SYSCLK until OC becomes "1". Then the HX8312-A writes the number of positive edges of SYSCLK (tcal) in the line clock register (R139). When LTS (D1 bit of the R1) is "1", the double number of the counted positive edges (tcalx2) will be set to R139.

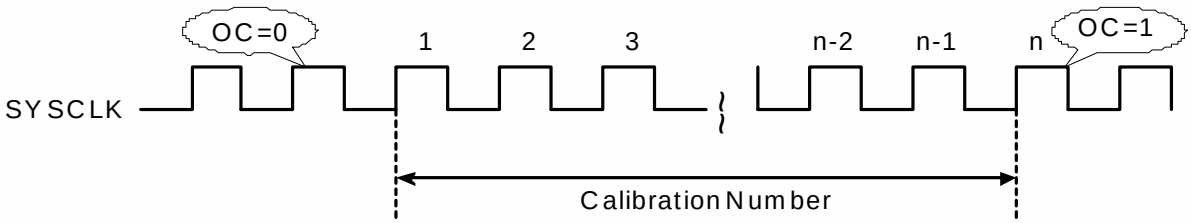


Figure 3. 9 Adjust by Calibration

3.3.2. Adjusting the one horizontal line period by register set-up

First users need to specify the target frame frequency, which will drive the LCD (60 Hz commonly.) Next using the formula below, calculate the integer of HCK, so that it is close to the target frame frequency.

$$Frame\ Frequency = \frac{SYSCLK}{HCK \times (GL + 1)}$$

SYSCLK	:	System clock frequency
HCK	:	Raster-row clock number
GL+1	:	Gate drive number (320) + 1 (dummy output)

Example:

$$60\ Hz = \frac{1200000\ Hz}{HCK \times (320 + 1)}$$

$$HCK = \frac{1200000}{60 \times 321} = 62.3$$

Please determine a value around HCK = 62 or 63 while drive the LCD with frame rate 60Hz. Remind that the setting in R139 can not be setting without the setting CLKM = “1”, therefore the default setting of HCK=”25”h stays valid.

Please note that the value in R139 must be ≥ “20”h.

4. Display RAM

The HX8312-A have an internal graphics RAM that stores 1,382,400-bits data, where one pixel is expressed by 18 bits. By specifying arbitrary X and Y address, it is possible to access the display RAM.

The bit allocation of a pixel in the display RAM is as below.

Bit	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Allocation	R-Dot						G-Dot						B-Dot					
	One Pixel																	

Figure 4. 1 Bit Allocation of a Pixel in the display RAM

4.1 Relation between the Display RAM Address and the Source Output Channel

The X size of display can be changed by setting NSO1-0 (D2-1 bits of R13).

R13		X Size
NSO1	NSO0	
0	0	240
0	1	208
1	0	180
1	1	Inhibited

Table 4. 1 X Size of Display Setting

When the X size is set as 208, the valid X addresses of the display RAM are from "00"h to "CF"h. Addresses "D0"h to "EF"h are invalid. Source outputs S313 to S408 are also invalid. When the X size is set as 180, the valid X addresses of the display data RAM are from "00"h to "B3"h. Addresses "B4"h to "EF"h are invalid. Source outputs S271 to S450 are also invalid.

By the ADC bit (D5 bit of R0) , the relation between the source output channel and the display data RAM address can be changed as reverse display. By setting the BGR bit (D0 bit of R193), the relation between the source output channel and the <R>,<G>,<B> dot allocation can be reversed for different LCD color filter arrangement. Table 4. 2, 4. 3 and 4.4 show relation between the display RAM data allocation, the R,G,B dot allocation and the source output channel.

BGR = 0														
Source Output	ADC = 0	S1	S2	S3	S4	S5	S6	-------	S715	S716	S717	S718	S719	S720
	ADC = 1	S718	S719	S720	S715	S716	S717	-------	S4	S5	S6	S1	S2	S3
X Address		“00”h			“01”h			-------	“EE”h			“EF”h		
Bit Allocation		17-12	11-6	5-0	17-12	11-6	5-0	-------	17-12	11-6	5-0	17-12	11-6	5-0
Pixel		Pixel 1			Pixel 2			-------	Pixel 239			Pixel 240		

BGR = 1														
Source Output	ADC = 0	S3	S2	S1	S6	S5	S4	-------	S717	S716	S715	S720	S719	S718
	ADC = 1	S720	S719	S718	S717	S716	S715	-------	S6	S5	S4	S3	S2	S1
X Address		“00”h			“01”h			-------	“EE”h			“EF”h		
Bit Allocation		17-12	11-6	5-0	17-12	11-6	5-0	-------	17-12	11-6	5-0	17-12	11-6	5-0
Pixel		Pixel 1			Pixel 2			-------	Pixel 239			Pixel 240		

Table 4. 2 Display RAM X Address and Display Panel Position (X Size = 240)

BGR = 0														
Source Output	ADC = 0	S1	S2	S3	S4	S5	S6	-------	S715	S716	S717	S718	S719	S720
	ADC = 1	S718	S719	S720	S715	S716	S717	-------	S4	S5	S6	S1	S2	S3
X Address		“00”h			“01”h			-------	“CE”h			“CF”h		
Bit Allocation		17-12	11-6	5-0	17-12	11-6	5-0	-------	17-12	11-6	5-0	17-12	11-6	5-0
Pixel		Pixel 1			Pixel 2			-------	Pixel 207			Pixel 208		

BGR = 1														
Source Output	ADC = 0	S3	S2	S1	S6	S5	S4	-------	S717	S716	S715	S720	S719	S718
	ADC = 1	S720	S719	S718	S717	S716	S715	-------	S6	S5	S4	S3	S2	S1
X Address		“00”h			“01”h			-------	“CE”h			“CF”h		
Bit Allocation		17-12	11-6	5-0	17-12	11-6	5-0	-------	17-12	11-6	5-0	17-12	11-6	5-0
Pixel		Pixel 1			Pixel 2			-------	Pixel 207			Pixel 208		

S313 to S408 are invalid

Table 4. 3 Display RAM X Address and Display Panel Position (X Size = 208)

BGR = 0														
Source Output	ADC = 0	S1	S2	S3	S4	S5	S6	-------	S715	S716	S717	S718	S719	S720
	ADC = 1	S718	S719	S720	S715	S716	S717	-------	S4	S5	S6	S1	S2	S3
X Address		“00”h			“01”h			-------	“B2”h			“B3”h		
Bit Allocation		17-12	11-6	5-0	17-12	11-6	5-0	-------	17-12	11-6	5-0	17-12	11-6	5-0
Pixel		Pixel 1			Pixel 2			-------	Pixel 179			Pixel 180		

BGR = 1														
Source Output	ADC = 0	S3	S2	S1	S6	S5	S4	-------	S717	S716	S715	S720	S719	S718
	ADC = 1	S720	S719	S718	S717	S716	S715	-------	S6	S5	S4	S3	S2	S1
X Address		“00”h			“01”h			-------	“B2”h			“B3”h		
Bit Allocation		17-12	11-6	5-0	17-12	11-6	5-0	-------	17-12	11-6	5-0	17-12	11-6	5-0
Pixel		Pixel 1			Pixel 2			-------	Pixel 179			Pixel 180		

S271 to S450 are invalid

Table 4. 4 Display RAM X Address and Display Panel Position (X Size = 180)

S/G pins	S1	S2	S3	S4	S5	S6	S7	S8	S9	---	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
	17---------0			17---------0			17---------0			---	17---------0			17---------0			17---------0			17---------0		
G1	0000h			0001h			0002h			---	00ECh			00EDh			00EEh			00EFh		
G2	0100h			0101h			0102h			---	01ECh			01EDh			01EEh			01EFh		
G3	0200h			0201h			0202h			---	02ECh			02EDh			02EEh			02EFh		
G4	0300h			0301h			0302h			---	03ECh			03EDh			03EEh			03EFh		
G5	0400h			0401h			0402h			---	04ECh			04EDh			04EEh			04EFh		
G6	0500h			0501h			0502h			---	05ECh			05EDh			05EEh			05EFh		
G7	0600h			0601h			0602h			---	06ECh			06EDh			06EEh			06EFh		
G8	0700h			0701h			0702h			---	07ECh			07EDh			07EEh			07EFh		
G9	0800h			0801h			0802h			---	08ECh			08EDh			08EEh			08EFh		
G10	0900h			0901h			0902h			---	09ECh			09EDh			09EEh			09EFh		
G11	0A00h			0A01h			0A02h			---	0AECh			0AEDh			0AEEh			0AEFh		
G12	0B00h			0B01h			0B02h			---	0BECh			0BEDh			0BEEh			0BEFh		
G13	0C00h			0C01h			0C02h			---	0CECh			0CEDh			0CEEh			0CEFh		
G14	0D00h			0D01h			0D01h				0DECh			0DEDh			0DEEh			0DEFh		
G15	0E00h			0E01h			0E01h				0EECh			0EEDh			0EEEh			0EEFh		
⋮	⋮			⋮			⋮			---	⋮			⋮			⋮			⋮		
G231	13600h			13601h			13602h			---	136ECh			136EDh			136EEh			136EFh		
G232	13700h			13701h			13702h			---	137ECh			137EDh			137EEh			137EFh		
G233	13800h			13801h			13802h			---	138ECh			138EDh			138EEh			138EFh		
G234	13900h			13901h			13902h			---	139ECh			139EDh			139EEh			139EFh		
G235	13A00h			13A01h			13A02h			---	13AECh			13AEDh			13AEEh			13AEFh		
G236	13B00h			13B01h			13B02h			---	13BECh			13BEDh			13BEEh			13BEFh		
G237	13C00h			13C01h			13C02h			---	13CECh			13CEDh			13CEEh			13CEFh		
G238	13D00h			13D01h			13D02h			---	13DECh			13DEDh			13DEEh			13DEFh		
G239	13E00h			13E01h			13E02h			---	13EECh			13EEDh			13EEEh			13EEFh		
G240	13F00h			13F01h			13F02h			---	13FECh			13FEDh			13FEEh			13FEFh		

Table 4. 5 Display RAM Address and Display Panel Position (X Size = 240, ADX = 0)

4.2 Display RAM Access

The HX8312-A contains a display RAM bus address counter (AC) which assigns X (pixel), Y(line) address for writing pixel data to display RAM. One X address equals to one pixel allocation. The display data will be written at a pixel which address is specified by X address register (R66) and Y address register 1, 2 (R67, R68). Every time when a pixel data is written into or read from the display RAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register bits AM(D2 bit of R5), ADX(D7 bit of R1) and ADR(D6 bit of R1) setting.

ADX	X Address Direction		
	X Size = 180	X Size = 208	X Size = 240
0	X0 **à** X179 **à** X0	X0 **à** X207 **à** X0	X0 **à** X239 **à** X0
1	X179 **à** X0 **à** X179	X207 **à** X0 **à** X207	X239 **à** X0 **à** X239

ADR	Y Address Direction
0	Y0 **à** Y319 **à** Y0
1	Y319 **à** Y0 **à** Y319

Table 4. 6 X Address and Y Address Update Direction Setting

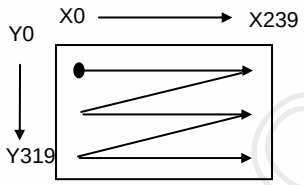
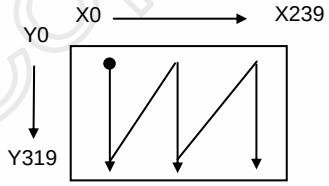
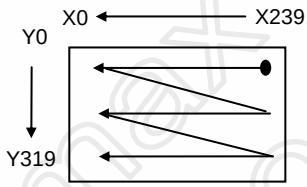
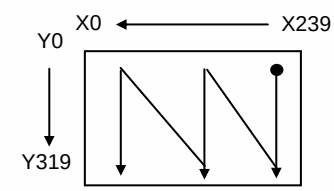
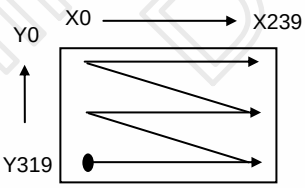
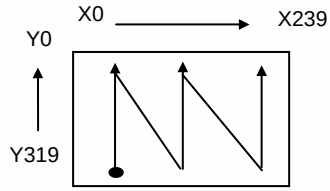
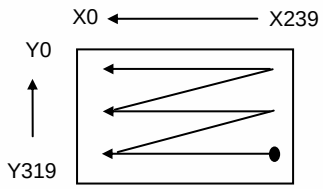
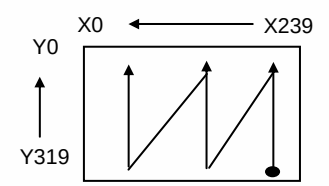
AM	ADR	ADX	Description Figure	AM	ADR	ADX	Description Figure
0	0	0		1	0	0	
		1				1	
	1	0			1	0	
		1				1	

Figure 4. 2 Address Update Direction Settings

4.3 Window Address Area Access Mode

To simplify the address control of display RAM access, the window area address function allows for writing data only within a window area of display RAM specified by registers. Setting WAS (D4 bit of data access control register R5) as “1” starts the window area access mode. After writing data to the display RAM, the AC will be increased or decreased within setting window address-range which is specified by the MIN X address (R69) and MAX X address register (R70) or the MIN Y address 1, 2(R71, R72) and MAX Y address 1, 2(R73, R74) register. Therefore, data can be written consecutively without thinking a data wrap by those bit function. When use window access mode, please make sure the following address setting restriction:

“00”h ≦ MIN X address ≦ X address ≦ MAX X address ≦ “EF”h
“00”h ≦ MIN Y address ≦ Y address ≦ MAX Y address ≦ “13F”h

The display RAM access address direction control still work in window access mode. In window access mode, the display RAM access X address boundary is restricted by R69 and R70 instead of X0 and X239 ; Y address boundary is restricted by R71,R72 and R73,R74 instead of Y0 and Y319.

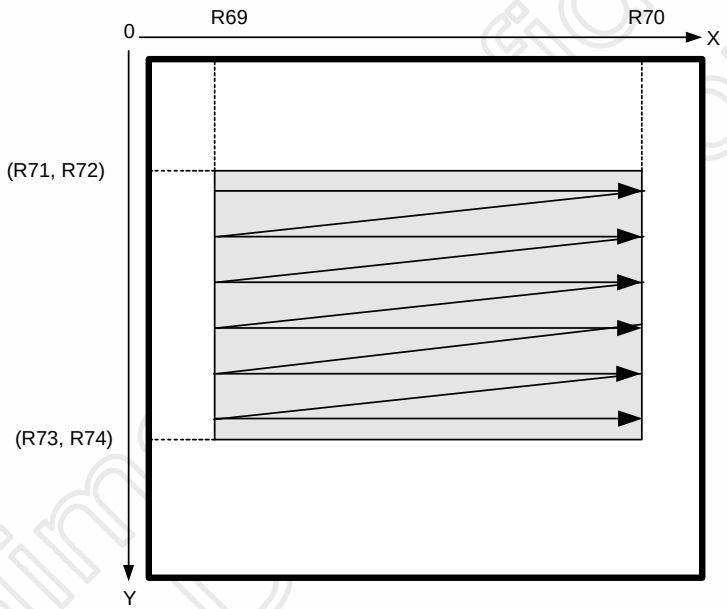
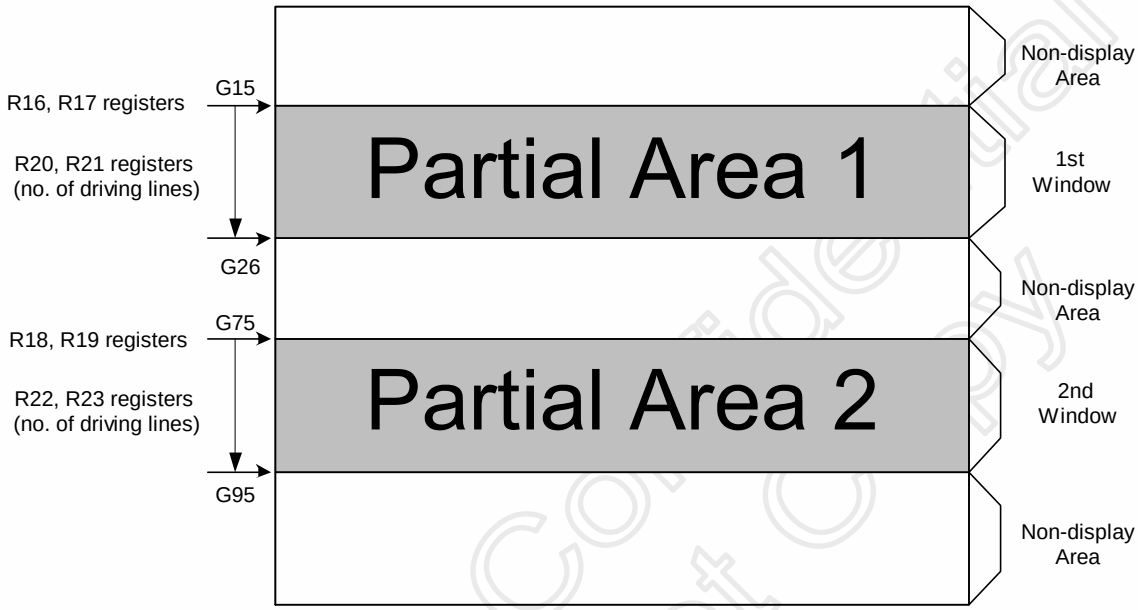


Figure 4. 3 Display RAM Access in Window Area Access Mode (AM=0, ADX=0, ADR=0)

5. Partial Display Mode

The HX8312-A enters a partial display mode when DTY (D4 bit of the control register 1 (R0)) is set as "1". The HX8312-A has one or two display window driving functions in partial display mode. The position of display screen register (R16-R23) can display at any line position of the whole screen. The numbers of display lines that display on the first and second display window must be less than total LCD-driving lines (320 lines). The number of the total selection driving lines included the 1st and 2nd display window must be equal to or less than the LCD Drive Line (320 lines).



Number of Scan Line: 320 lines
Ex: 1st Screen Setting: (R16, R17) = “0E”h, (R20, R21) = “0B”h
2nd Screen Setting: (R18, R19) = “4A”h, (R22, R23) = “14”h

Figure 5. 1 Partial Screen Display Example in 2-Windows Driving

Note: 1. The start driving line of partial areas are ((R16, R17) + 1) line for the first display window and ((R18, R19) +1) for second display window.
2. Please make sure the conditions. (R16, R17 + R20, R21) <320 , (R18, R19 + R22, R23) < 320.
3. For only one display window display operation, it can be set the same value in (R16,R17) , (R18,R19) and (R20,R21) , (R22,R23).
4. That incorrect display may occur if the condition setting is not matched the spec.

The following table shows the register for first and second display window area setting in partial display mode.

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	-	-	P1SL8

Table 5. 1 First display window area starting register 1 (R16)

D7	D6	D5	D4	D3	D2	D1	D0
P1SL7	P1SL6	P1SL5	P1SL4	P1SL3	P1SL2	P1SL1	P1SL0

Table 5. 2 First display window area starting register 2 (R17)

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	-	-	P2SL8

Table 5. 3 Second display window area starting register 1 (R18)

D7	D6	D5	D4	D3	D2	D1	D0
P2SL7	P2SL6	P2SL5	P2SL4	P2SL3	P2SL2	P2SL1	P2SL0

Table 5. 4 Second display window starting register 2 (R19)

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	-	-	P1AW8

Table 5. 5 First display window area driving line number register 1 (R20)

D7	D6	D5	D4	D3	D2	D1	D0
P1AW7	P1AW6	P1AW5	P1AW4	P1AW3	P1AW2	P1AW1	P1AW0

Table 5. 6 First display window area display line number register 2 (R21)

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	-	-	P2AW8

Table 5. 7 Second display window area display line number register 1 (R22)

D7	D6	D5	D4	D3	D2	D1	D0
P2AW7	P2AW6	P2AW5	P2AW4	P2AW3	P2AW2	P2AW1	P2AW0

Table 5. 8 Second display window area display line number register 2 (R23)

5.1 Display Color Selection and Gate Scan Method in Partial Non-Display Areas

The color of non-display areas is specified by the partial non-display area color register 1 (R14) and the partial non-display area color register 2 (R15).

PSEL (D0 bit of R14)	PGR, PGG, PGB (D2-0 bits of R15)	Display Color in non-Display Area
0	“000”	Black
	“001”	Red
	“010”	Green
	“011”	Yellow
	“100”	Blue
	“101”	Purple
	“110”	Cyan
	“111”	White
1	-	Display the most significant bit of each display data in display RAM.

Table 5. 9 Display Color in non-Display Areas of Partial Display Mode

The gate scan method in of partial non-display areas can be selected by setting PNFRM (D0 bit of R53) as follow.

Gate Scan of Display Area	Gate Scan of Partial non-Display Area	
	PNFRM = 0	PNFRM = 1
Frame Inversion Driving	Frame Inversion Driving	Frame Inversion Driving
N-Line Inversion Driving	N-Line Inversion Driving.	Frame Inversion Driving
3-field Interlaced Driving	3-field Interlaced Driving	

Table 5. 10 Gate Scan Method in non-Display Areas of Partial Display Mode

Arbitrary frame refresh scan: (Inhibited to use)

Arbitrary frame refresh scan can be available in partial non-display area when frame inversion or N-line inversion driving scan is selected in display areas of partial display mode. By setting GSM (D0 bit of the control register 1, R0) as "1" and GSMLN7-0 (D7-0 bits of the partial gate register 1 , R52) are used to define the number of frame which gate scan will be performed in partial non-display area.

Please note that when GSMLN7-0 is set as "00h", no gate scan will be performed in the partial non-display areas.

GSMLN7	GSMLN6	GSMLN5	GSMLN4	GSMLN3	GSMLN2	GSMLN1	GSMLN0	Refresh frame number
0	0	0	0	0	0	0	0	Gate scan always stop
0	0	0	0	0	0	0	1	Every 1 frame
0	0	0	0	0	0	1	0	Every 2 frame
				•				
				•				
1	1	1	1	1	1	1	0	Every 254 frame
1	1	1	1	1	1	1	1	Every 255 frame

Table 5. 11 Partial gate register 1 (R52)

6. Vertical Scroll Function

The HX8312-A incorporates a scroll display function, which performs a scroll display operation without repudiating display RAM for reducing chip RAM access. Since this scroll function is not automatic, please follow the instructions below to operate this function manually.

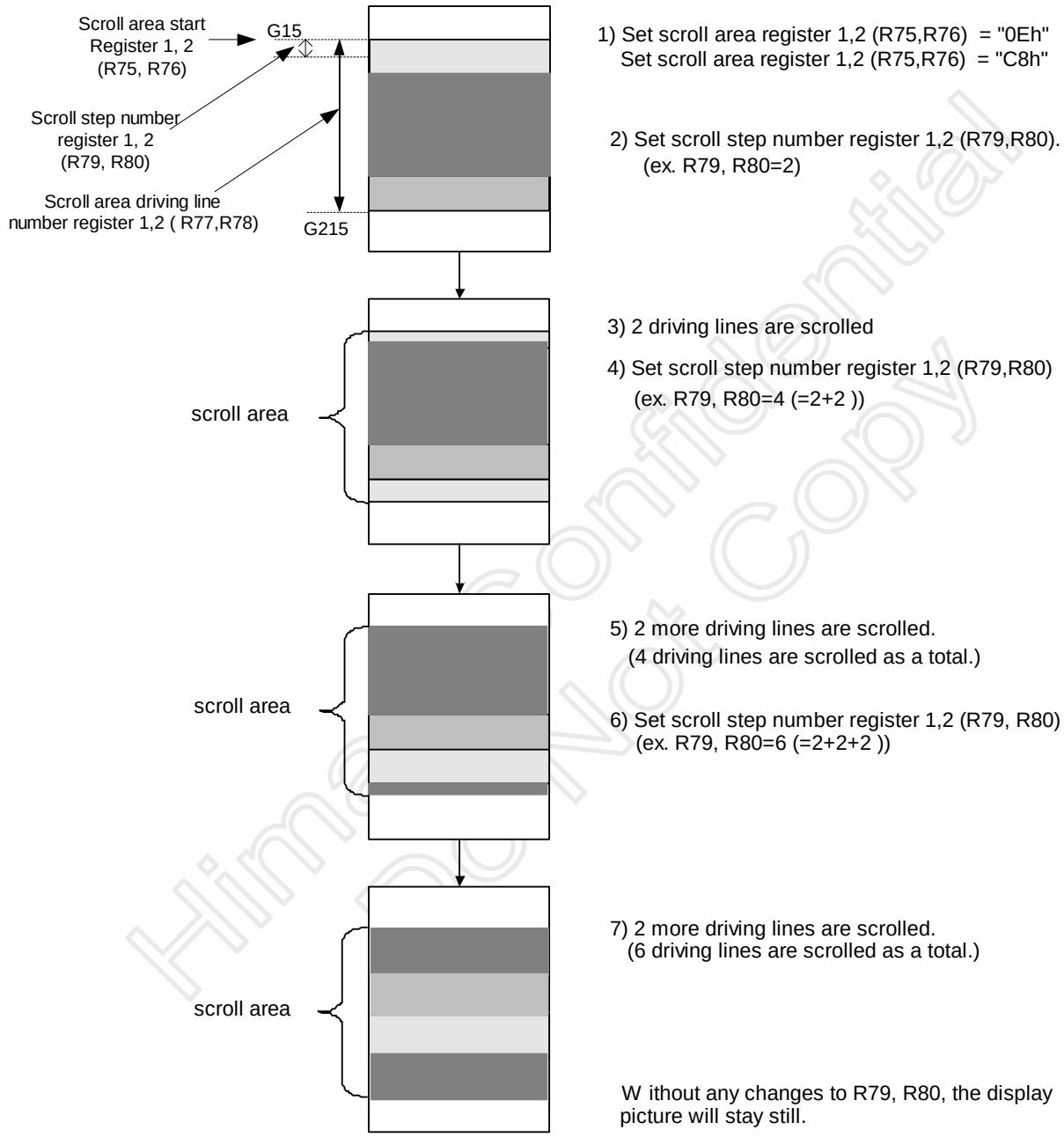


Figure 6. 1 Scroll Function Driving

To go back to the display before scrolling, please set the scroll step number register1,2 (R79, R80) as "000"h. Please make sure to set the number of driving lines to be scrolled (set value of R79 and R80) less than the line number of the scroll area. When the value of R79, R80 exceeds the value of R77 and R78, please set new value which is less than R77 and R78 again to R79 and R80.

SSL8	SSL7	SSL6	SSL5	SSL4	SSL3	SSL2	SSL1	SSL0	Raster-row start address
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	1	1	3
. .									. .
1	0	0	1	1	1	1	0	1	317
1	0	0	1	1	1	1	1	0	318
1	0	0	1	1	1	1	1	1	319

Table 6. 1 Scroll Area Start Register 1, 2 (R75, R76)

SAW8	SAW7	SAW6	SAW5	SAW4	SAW3	SAW2	SAW1	SAW0	Scroll area driving line number
0	0	0	0	0	0	0	0	0	Setting Inhibited
0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	1	1	3
. .					. .				
1	0	0	1	1	1	1	0	1	317
1	0	0	1	1	1	1	1	0	318
1	0	0	1	1	1	1	1	1	319

Table 6. 2 Scroll Area Driving Line Number Register 1, 2 (R77, R78)

SST8	SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0	Scroll step number
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	1	1	3
. .									. .
1	0	0	1	1	1	1	0	1	317
1	0	0	1	1	1	1	1	0	318
1	0	0	1	1	1	1	1	1	319

Table 6. 3 Scroll Step Number Register 1, 2 (R79, R80)

7. Gate Line Driving Function

Table 7. 1 shows the available gate line driving modes of the HX8312-A. Please set it up according to users' panel's characteristics.

LCD driving mode	GSCAN2 R55:D2	GSCAN1 R55:D1	GSCAN0 R55:D0	Description
Frame Inversion	0	0	0	The polarity of VCOM output is alternated once every frame.
N Line Inversion	0	0	1	The polarity of VCOM output is alternated once N line which N is defined by R51.
3-field Interlaced	1	1	0	Divided one frame scan into 3-field scan, and the polarity of VCOM output is alternated once every field.

Table 7. 1 Gate Line Driving Mode

The HX8312-A has an interlaced driving function that divided one frame scan into 3 fields scan for flicker-free display. As following Figure, by setting GSCAN2-0 = "111" (D2-0 bits of R55) the gate scan order of one frame is changed to
G1 **à** G4 **à** G7 **à**….. **à** G319 **à** G2 **à** G5 **à** G8 **à**…..**à**G320 **à** G3 **à** G6 **à** G9 **à**…..**à** G321
(3-field interlaced driving)

GSCAN2-0	111		
Field / Gate	1	2	3
G1	·		
G2		·	
G3			·
G4	·		
G5		·	
G6			·
G7	·		
G8		·	
G9			·
:	:	:	:
G318			
G319	·		
G320		·	
G321			·

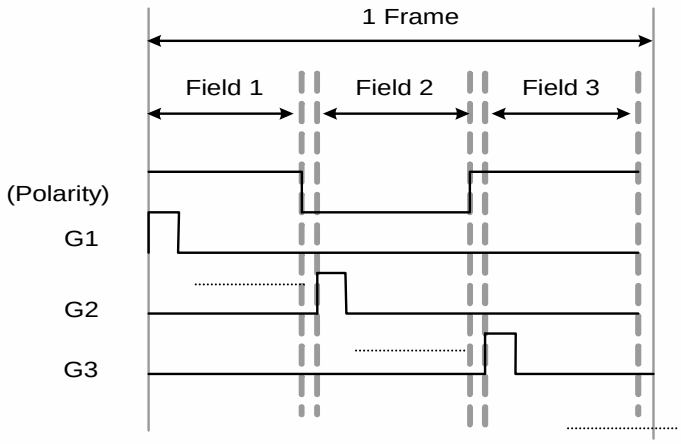


Figure 7. 1 Output Timing for Interlaced Gate Signals (Three-Field is selected)

The polarity of VCOM output in every driving mode is as follow:

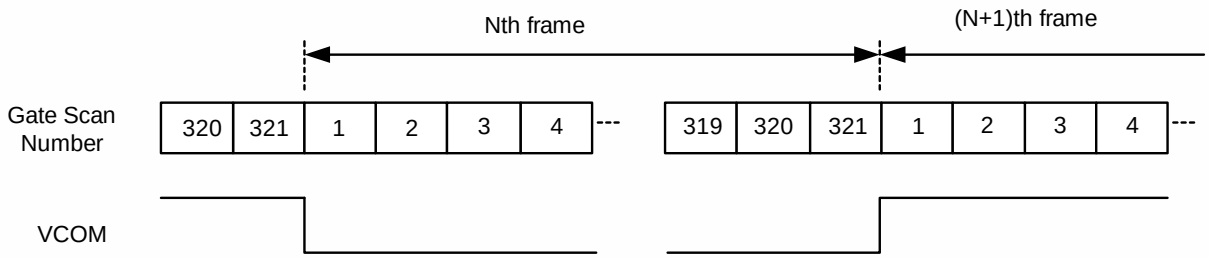


Figure 7. 2 Frame inversion LCD Driving

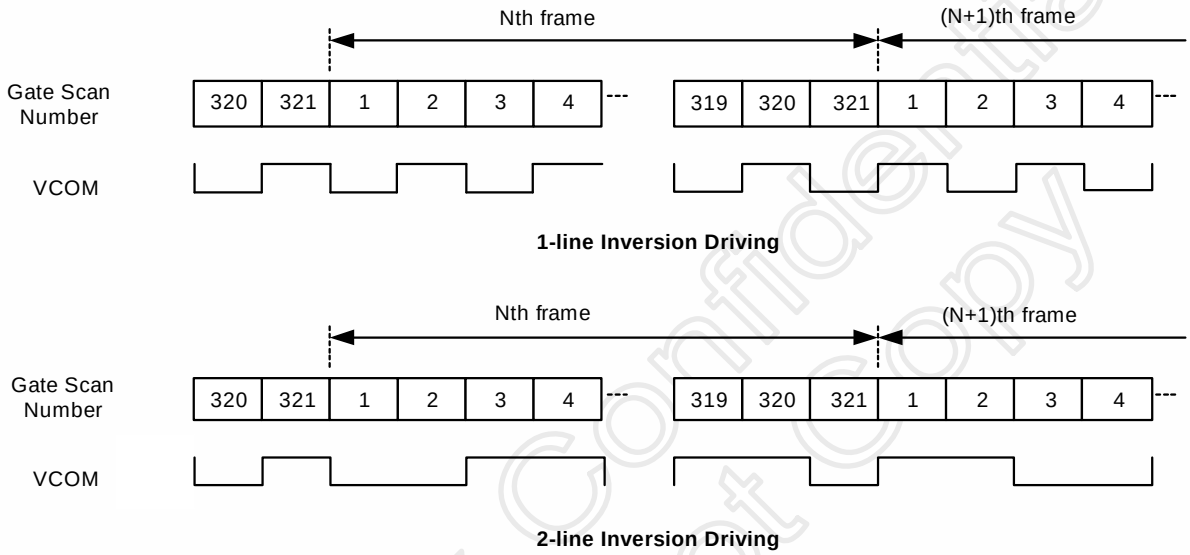


Figure 7. 3 N-line inversion LCD Driving

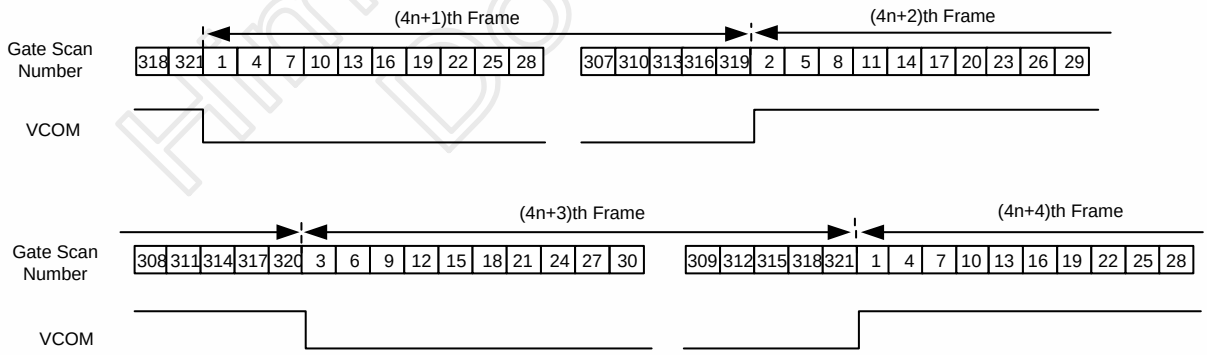


Figure 7. 4 3-field Interlaced LCD Driving

8. Gamma Adjustment Function

The HX8312-A incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. Then total 64 grayscale levels are generated in grayscale voltage generator. These registers are available for both polarities. However, R, G, B can not be adjusted individually.

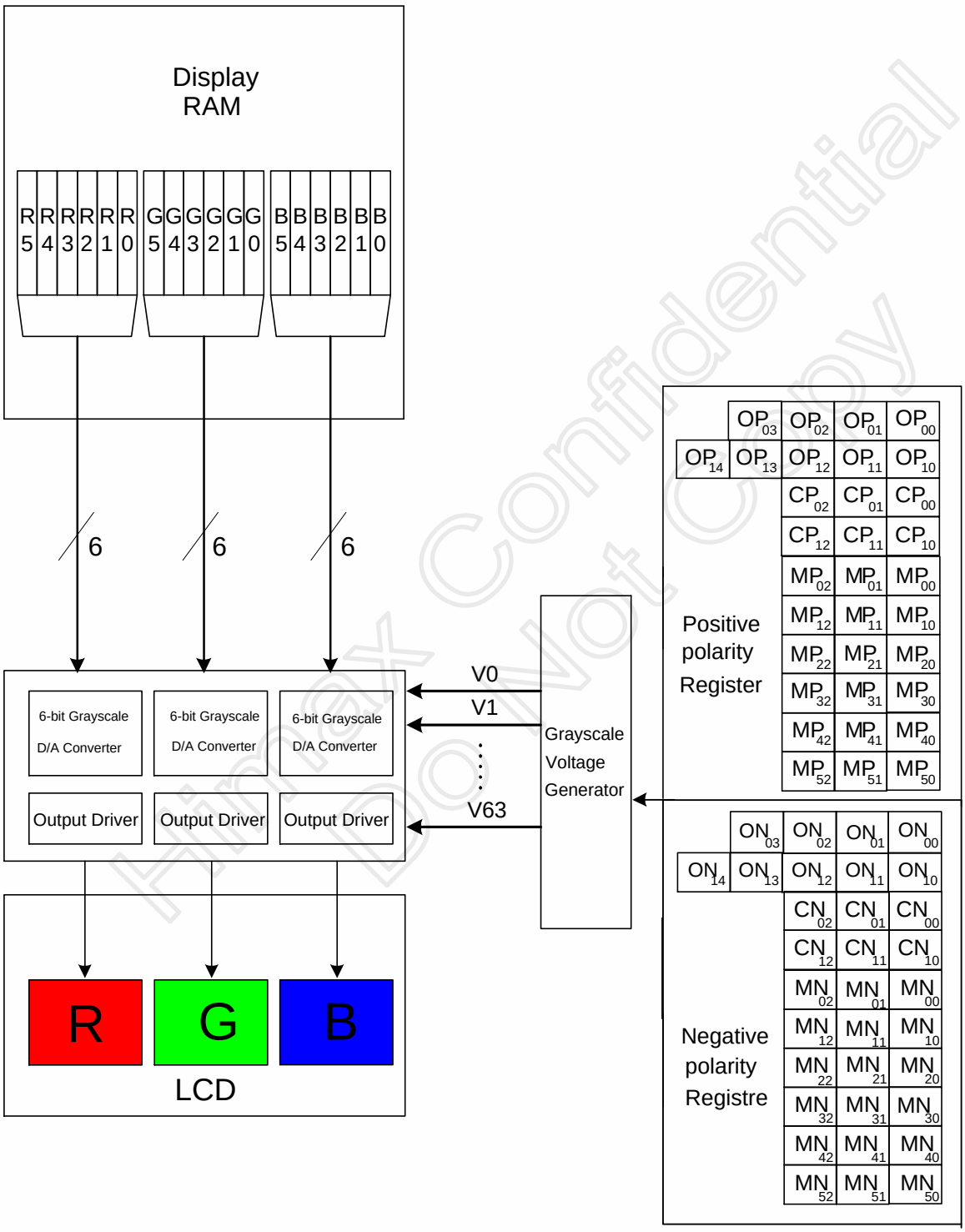


Figure 8. 1 Grayscale Control

8.1 Structure of Grayscale Voltage Generator

Eight reference gamma voltages VgP/N(0, 1, 8, 20, 43, 55, 62, 63) for positive and negative polarity are specified by the center adjustment, the micro adjustment and the offset adjustment registers firstly. With those eight voltage injected into specified node of grayscale voltage generator, total 64 grayscale voltages (V0-V63) can be generated from grayscale amplifier for LCD panel used.

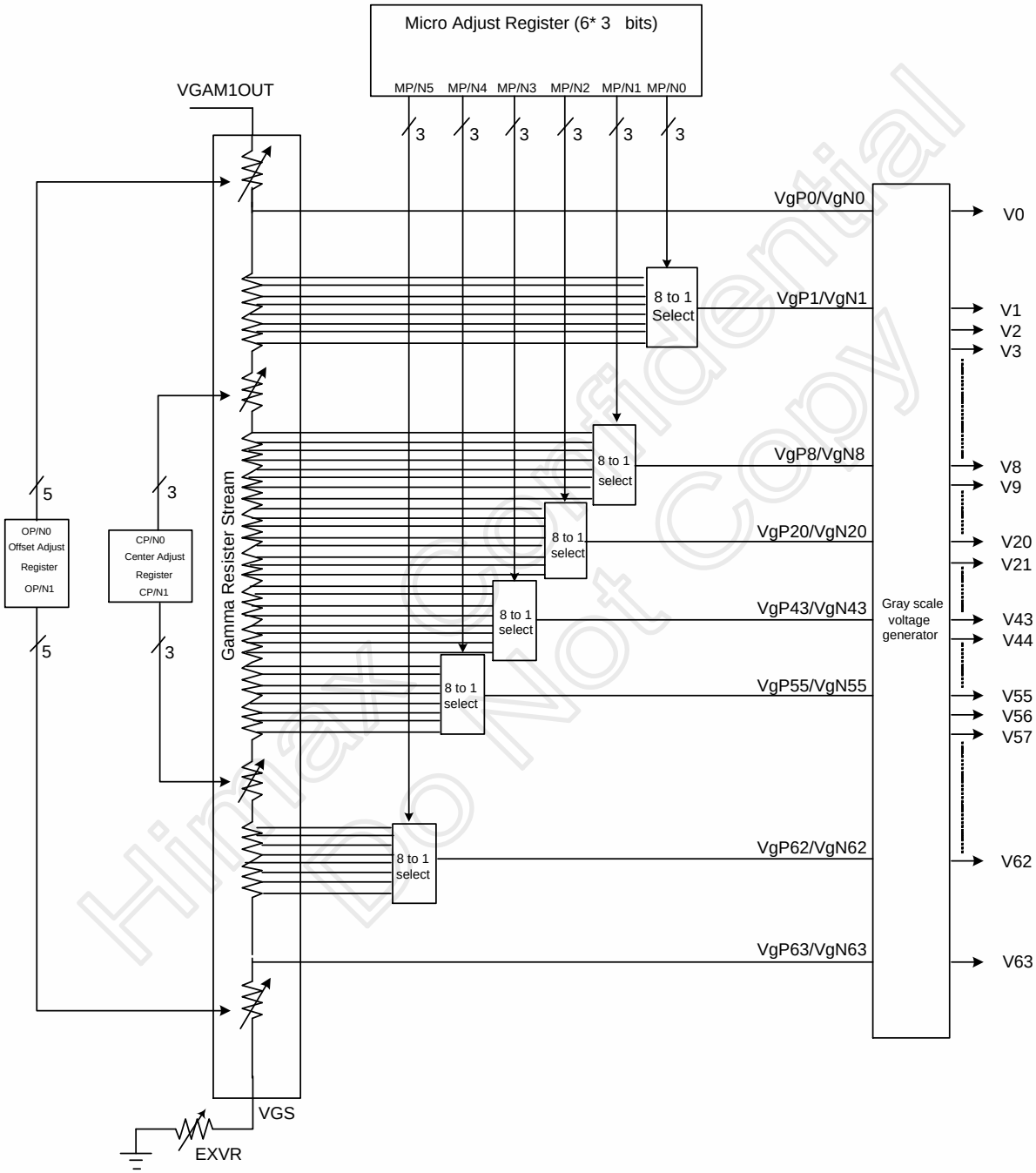


Figure 8. 2 Structure of Grayscale Voltage Generator

8.2 Gamma-Characteristics Adjustment Register

This HX8312-A has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently. (R, G, and B are common.)

(1)Gamma offset adjustment registers (R151, R152, R153, R154)

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

(2)Gamma center adjustment registers (R146, R150)

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 8 to 1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

(3)Gamma macro adjustment registers (R143, R144, R145, R147, R148, R149)

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 8-to-1 selectors (MP/N0~5), each of which has 8 inputs and generate one reference voltage output (VgP/N) 1, 8, 20, 43, 55, 62). These registers are available for both positive and negative polarities.

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	CP0 2-0	CN0 2-0	Variable resistor (VRCP/N0) for center adjustment
	CP1 2-0	CN1 2-0	Variable resistor (VRCP/N1)for center adjustment
Macro Adjustment	MP0 2-0	MN0 2-0	8-to-1 selector (voltage level of grayscale 1)
	MP1 2-0	MN1 2-0	8-to-1 selector (voltage level of grayscale 8)
	MP2 2-0	MN2 2-0	8-to-1 selector (voltage level of grayscale 20)
	MP3 2-0	MN3 2-0	8-to-1 selector (voltage level of grayscale 43)
	MP4 2-0	MN4 2-0	8-to-1 selector (voltage level of grayscale 55)
	MP5 2-0	MN5 2-0	8-to-1 selector (voltage level of grayscale 62)
Offset Adjustment	OP0 3-0	ON0 3-0	Variable resistor (VROP/N0)for offset adjustment
	OP1 4-0	ON1 4-0	Variable resistor (VROP/N1)for offset adjustment

Table 8. 1 Gamma-Adjustment Registers

8.3 Gamma Voltage Calculation Formula

Each circuit consists of two gamma resister streams one is for positive polarity and the other is for negative polarity, each one including eight gamma reference voltages. (VgP/N) 0, 1, 8, 20, 43, 55, 62, 63). Furthermore, the block has pin (VGS) to connect a variable resistor outside the chip for the variation between panels if needed.

8.3.1 Gamma Curve Adjustment Circuit

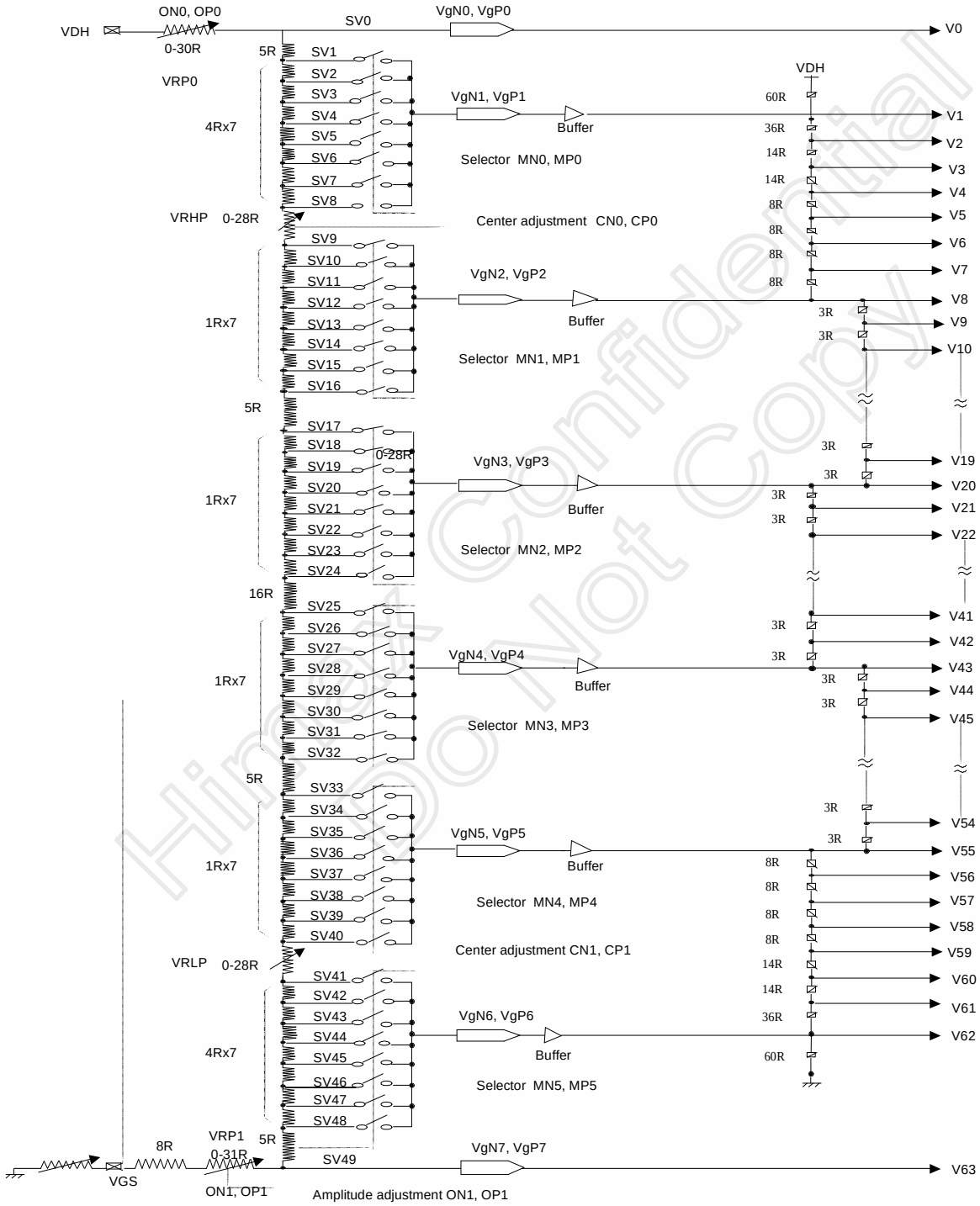


Figure 8. 3 Gamma Correction Circuit

8.3.2 Variable Resister

There are two types of variable resistors in gamma adjustment circuit, one is for center adjustment, and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

Value in Register O(P/N)0 3-0	Resistance	Value in Register O(P/N)1 4-0	Resistance	Value in Register C(P/N)0/1 2-0	Resistance
0000	0R	00000	0R	000	0R
0001	2R	00001	1R	001	4R
0010	4R	00010	2R	010	8R
• •	• •	• •	• •	011	12R
				100	16R
1101	26R	11101	29R	101	20R
1110	28R	11110	30R	110	24R
1111	30R	11111	31R	111	28R

Table 8. 2 Offset, Center, Adjustment Registers

8 to 1 Selector

The 8 to 1 selector has eight input voltages generated by gamma resister stream. It outputs one reference voltages selected from inputs for gamma reference voltage generation by setting value in macro adjustment register. These six 8 to 1 selectors and the relationship are shown below.

Value in Register	Voltage level					
M(P/N) 2-0	Vg(N/P) 1	Vg(N/P) 8	Vg(N/P) 20	Vg(N/P) 43	Vg(N/P) 55	Vg(N/P) 62
000	SV1	SV9	SV17	SV25	SV33	SV41
001	SV2	SV10	SV18	SV26	SV34	SV42
010	SV3	SV11	SV19	SV27	SV35	SV43
011	SV4	SV12	SV20	SV28	SV36	SV44
100	SV5	SV13	SV21	SV29	SV37	SV45
101	SV6	SV14	SV22	SV30	SV38	SV46
110	SV7	SV15	SV23	SV31	SV39	SV47
111	SV8	SV16	SV24	SV32	SV40	SV48

Table 8. 3 Output Voltage of 8 to 1 Selector

8.3.3 The grayscale levels are determined by the following formulas

Reference Voltage	Adjustment Register -- Positive	Adjustment Register -- Negative	Formula	Voltage
VgN/P0	---	---	VDH – DV × VR0 / SUMR	SV0
VgN/P1	MP0 2-0=000	MN0 2-0=000	VDH – DV × (VR0 +5R) / SUMR	SV1
	MP0 2-0=001	MN0 2-0=001	VDH – DV × (VR0 +9R) / SUMR	SV2
	MP0 2-0=010	MN0 2-0=010	VDH – DV × (VR0 +13R) / SUMR	SV3
	MP0 2-0=011	MN0 2-0=011	VDH – DV × (VR0 +17R) / SUMR	SV4
	MP0 2-0=100	MN0 2-0=100	VDH – DV × (VR0 +21R) / SUMR	SV5
	MP0 2-0=101	MN0 2-0=101	VDH – DV × (VR0 +25R) / SUMR	SV6
	MP0 2-0=110	MN0 2-0=110	VDH – DV × (VR0 +29R) / SUMR	SV7
	MP0 2-0=111	MN0 2-0=111	VDH – DV × (VR0 +33R) / SUMR	SV8
VgN/P8	MP1 2-0=000	MN1 2-0=000	VDH – DV × (VR0 +33R + VRH) / SUMR	SV9
	MP1 2-0=001	MN1 2-0=001	VDH – DV × (VR0 +34R + VRH) / SUMR	SV10
	MP1 2-0=010	MN1 2-0=010	VDH – DV × (VR0 +35R + VRH) / SUMR	SV11
	MP1 2-0=011	MN1 2-0=011	VDH – DV × (VR0 +36R + VRH) / SUMR	SV12
	MP1 2-0=100	MN1 2-0=100	VDH – DV × (VR0 +37R + VRH) / SUMR	SV13
	MP1 2-0=101	MN1 2-0=101	VDH – DV × (VR0 +38R + VRH) / SUMR	SV14
	MP1 2-0=110	MN1 2-0=110	VDH – DV × (VR0 +39R + VRH) / SUMR	SV15
	MP1 2-0=111	MN1 2-0=111	VDH – DV × (VR0 +40R + VRH) / SUMR	SV16
VgN/P20	MP2 2-0=000	MN2 2-0=000	VDH – DV × (VR0 +45R + VRH) / SUMR	SV17
	MP2 2-0=001	MN2 2-0=001	VDH – DV × (VR0 +46R + VRH) / SUMR	SV18
	MP2 2-0=010	MN2 2-0=010	VDH – DV × (VR0 +47R + VRH) / SUMR	SV19
	MP2 2-0=011	MN2 2-0=011	VDH – DV × (VR0 +48R + VRH) / SUMR	SV20
	MP2 2-0=100	MN2 2-0=100	VDH – DV × (VR0 +49R + VRH) / SUMR	SV21
	MP2 2-0=101	MN2 2-0=101	VDH – DV × (VR0 +50R + VRH) / SUMR	SV22
	MP2 2-0=110	MN2 2-0=110	VDH – DV × (VR0 +51R + VRH) / SUMR	SV23
	MP2 2-0=111	MN2 2-0=111	VDH – DV × (VR0 +52R + VRH) / SUMR	SV24
VgN/P43	MP3 2-0=000	MN3 2-0=000	VDH – DV × (VR0 +68R + VRH) / SUMR	SV25
	MP3 2-0=001	MN3 2-0=001	VDH – DV × (VR0 +69R + VRH) / SUMR	SV26
	MP3 2-0=010	MN3 2-0=010	VDH – DV × (VR0 +70R + VRH) / SUMR	SV27
	MP3 2-0=011	MN3 2-0=011	VDH – DV × (VR0 +71R + VRH) / SUMR	SV28
	MP3 2-0=100	MN3 2-0=100	VDH – DV × (VR0 +72R + VRH) / SUMR	SV29
	MP3 2-0=101	MN3 2-0=101	VDH – DV × (VR0 +73R + VRH) / SUMR	SV30
	MP3 2-0=110	MN3 2-0=110	VDH – DV × (VR0 +74R + VRH) / SUMR	SV31
	MP3 2-0=111	MN3 2-0=111	VDH – DV × (VR0 +75R + VRH) / SUMR	SV32
VgN/P55	MP4 2-0=000	MN4 2-0=000	VDH – DV × (VR0 +80R + VRH) / SUMR	SV33
	MP4 2-0=001	MN4 2-0=001	VDH – DV × (VR0 +81R + VRH) / SUMR	SV34
	MP4 2-0=010	MN4 2-0=010	VDH – DV × (VR0 +82R + VRH) / SUMR	SV35
	MP4 2-0=011	MN4 2-0=011	VDH – DV × (VR0 +83R + VRH) / SUMR	SV36
	MP4 2-0=100	MN4 2-0=100	VDH – DV × (VR0 +84R + VRH) / SUMR	SV37
	MP4 2-0=101	MN4 2-0=101	VDH – DV × (VR0 +85R + VRH) / SUMR	SV38
	MP4 2-0=110	MN4 2-0=110	VDH – DV × (VR0 +86R + VRH) / SUMR	SV39
	MP4 2-0=111	MN4 2-0=111	VDH – DV × (VR0 +87R + VRH) / SUMR	SV40
VgN/P62	MP5 2-0=000	MN5 2-0=000	VDH – DV × (VR0 +87R + VRH +VRL) / SUMR	SV41
	MP5 2-0=001	MN5 2-0=001	VDH – DV × (VR0 +91R + VRH +VRL) / SUMR	SV42
	MP5 2-0=010	MN5 2-0=010	VDH – DV × (VR0 +95R + VRH +VRL) / SUMR	SV43
	MP5 2-0=011	MN5 2-0=011	VDH – DV × (VR0 +99R + VRH +VRL) / SUMR	SV44
	MP5 2-0=100	MN5 2-0=100	VDH – DV × (VR0 +103R + VRH +VRL) / SUMR	SV45
	MP5 2-0=101	MN5 2-0=101	VDH – DV × (VR0 +107R + VRH +VRL) / SUMR	SV46
	MP5 2-0=110	MN5 2-0=110	VDH – DV × (VR0 +111R + VRH +VRL) / SUMR	SV47
	MP5 2-0=111	MN5 2-0=111	VDH – DV × (VR0 +115R + VRH +VRL) / SUMR	SV48
VgN/P63	---	---	VDH – DV × (VR0 +120R + VRH +VRL) / SUMR	SV49

Table 8. 4 Voltage Calculation Formula

Note: SUMR: Sum of ladder resistors = 128R + VRH + VRL + VR0 + VR1
DV: Voltage difference between VDH and VGS.

Grayscale Voltage	Formula
V0	VgN/P0
V1	VgN/P1
V2	V8+(V1-V8)*(30/48)
V3	V8+(V1-V8)*(23/48)
V4	V8+(V1-V8)*(16/48)
V5	V8+(V1-V8)*(12/48)
V6	V8+(V1-V8)*(8/48)
V7	V8+(V1-V8)*(4/48)
V8	VgN/P8
V9	V20+(V8-V20)*(22/24)
V10	V20+(V8-V20)*(20/24)
V11	V20+(V8-V20)*(18/24)
V12	V20+(V8-V20)*(16/24)
V13	V20+(V8-V20)*(14/24)
V14	V20+(V8-V20)*(12/24)
V15	V20+(V8-V20)*(10/24)
V16	V20+(V8-V20)*(8/24)
V17	V20+(V8-V20)*(6/24)
V18	V20+(V8-V20)*(4/24)
V19	V20+(V8-V20)*(2/24)
V20	VgN/P20
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)

Grayscale Voltage	Formula
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VgN/P43
V44	V55+(V43-V55)*(22/24)
V45	V55+(V43-V55)*(20/24)
V46	V55+(V43-V55)*(18/24)
V47	V55+(V43-V55)*(16/24)
V48	V55+(V43-V55)*(14/24)
V49	V55+(V43-V55)*(12/24)
V50	V55+(V43-V55)*(10/24)
V51	V55+(V43-V55)*(8/24)
V52	V55+(V43-V55)*(6/24)
V53	V55+(V43-V55)*(4/24)
V54	V55+(V43-V55)*(2/24)
V55	VgN/P55
V56	V62+(V55-V62)*(44/48)
V57	V62+(V55-V62)*(40/48)
V58	V62+(V55-V62)*(36/48)
V59	V62+(V55-V62)*(32/48)
V60	V62+(V55-V62)*(25/48)
V61	V62+(V55-V62)*(18/48)
V62	VgN/P62
V63	VgN/P63

Table 8. 5 Voltage Calculation Formula of Grayscale Voltage

Note: The following relationship should be retained.
VgN/P63 – GND > 0.3V

GRAM Data Set-up RGB	Selected Grayscale	
	P	N
000000	V0	V63
000001	V1	V62
000010	V2	V61
000011	V3	V60
000100	V4	V59
000101	V5	V58
000110	V6	V57
000111	V7	V56
001000	V8	V55
001001	V9	V54
001010	V10	V53
001011	V11	V52
001100	V12	V51
001101	V13	V50
001110	V14	V49
001111	V15	V48

GRAM Data Set-up RGB	Selected Grayscale	
	P	N
010000	V16	V47
010001	V17	V46
010010	V18	V45
010011	V19	V44
010100	V20	V43
010101	V21	V42
010110	V22	V41
010111	V23	V40
011000	V24	V39
011001	V25	V38
011010	V26	V37
011011	V27	V36
011100	V28	V35
011101	V29	V34
011110	V30	V33
011111	V31	V32

GRAM Data Set-up RGB	Selected Grayscale	
	P	N
100000	V32	V31
100001	V33	V30
100010	V34	V29
100011	V35	V28
100100	V36	V27
100101	V37	V26
100110	V38	V25
100111	V39	V24
101000	V40	V23
101001	V41	V22
101010	V42	V21
101011	V43	V20
101100	V44	V19
101101	V45	V18
101110	V46	V17
101111	V47	V16

GRAM Data Set-up RGB	Selected Grayscale	
	P	N
110000	V48	V15
110001	V49	V14
110010	V50	V13
110011	V51	V12
110100	V52	V11
110101	V53	V10
110110	V54	V9
110111	V55	V8
111000	V56	V7
111001	V57	V6
111010	V58	V5
111011	V59	V4
111100	V60	V3
111101	V61	V2
111110	V62	V1
111111	V63	V0

Table 8. 6 Display RAM Data and Grayscale Voltage Mapping (REV = 0 D0 bit of R6)

GRAM Data Set-up RGB	Selected Grayscale	
	P	N
000000	V63	V0
000001	V62	V1
000010	V61	V2
000011	V60	V3
000100	V59	V4
000101	V58	V5
000110	V57	V6
000111	V56	V7
001000	V55	V8
001001	V54	V9
001010	V53	V10
001011	V52	V11
001100	V51	V12
001101	V50	V13
001110	V49	V14
001111	V48	V15

GRAM Data Set-up RGB	Selected Grayscale	
	P	N
010000	V47	V16
010001	V46	V17
010010	V45	V18
010011	V44	V19
010100	V43	V20
010101	V42	V21
010110	V41	V22
010111	V40	V23
011000	V39	V24
011001	V38	V25
011010	V37	V26
011011	V36	V27
011100	V35	V28
011101	V34	V29
011110	V33	V30
011111	V32	V31

GRAM Data Set-up RGB	Selected Grayscale	
	P	N
100000	V31	V32
100001	V30	V33
100010	V29	V34
100011	V28	V35
100100	V27	V36
100101	V26	V37
100110	V25	V38
100111	V24	V39
101000	V23	V40
101001	V22	V41
101010	V21	V42
101011	V20	V43
101100	V19	V44
101101	V18	V45
101110	V17	V46
101111	V16	V47

GRAM Data Set-up RGB	Selected Grayscale	
	P	N
110000	V15	V48
110001	V14	V49
110010	V13	V50
110011	V12	V51
110100	V11	V52
110101	V10	V53
110110	V9	V54
110111	V8	V55
111000	V7	V56
111001	V6	V57
111010	V5	V58
111011	V4	V59
111100	V3	V60
111101	V2	V61
111110	V1	V62
111111	V0	V63

Table 8. 7 Display RAM Data and Grayscale Voltage Mapping (REV = 1)

8.3.4 Relationship between GRAM Data and Output Level

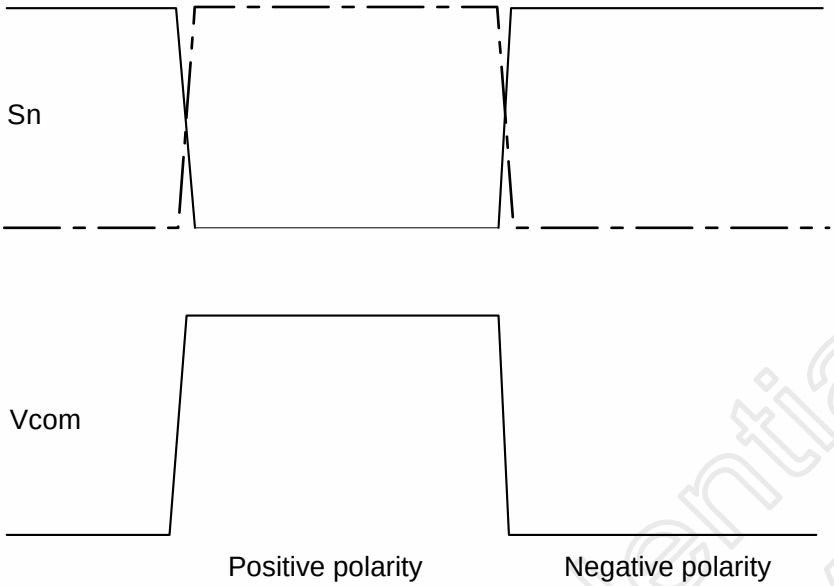
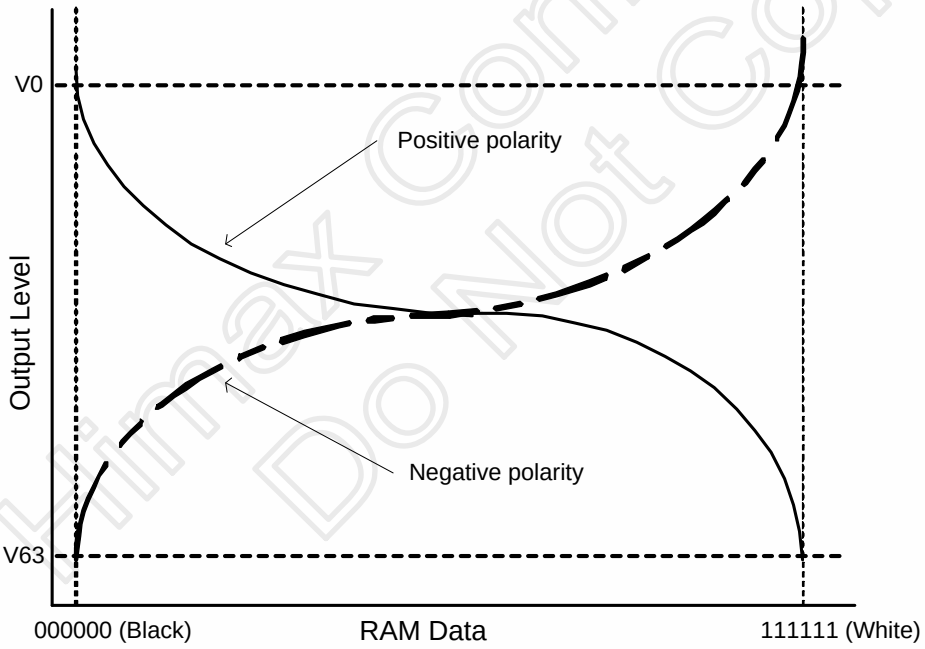


Figure 8. 4 Relationship between Source Output and Vcom



(Same characteristic for each RGB)

Figure 8. 5 Relationship between GRAM Data and Output Level (REV = 1)

9. 8–Color Display Mode Function

The HX8312-A supports an 8-color display mode by setting COLOR (D2 bit of R0) as “1”. The grayscale level to be used is V0 and V63 with R5, G5, B5 decoding, and the other levels (V1-V62) are halted to reduce power consumption in 8-color display mode. In 8-color display mode, the Gamma-micro-adjustment registers are invalid and only the upper bits of RGB are used for display.

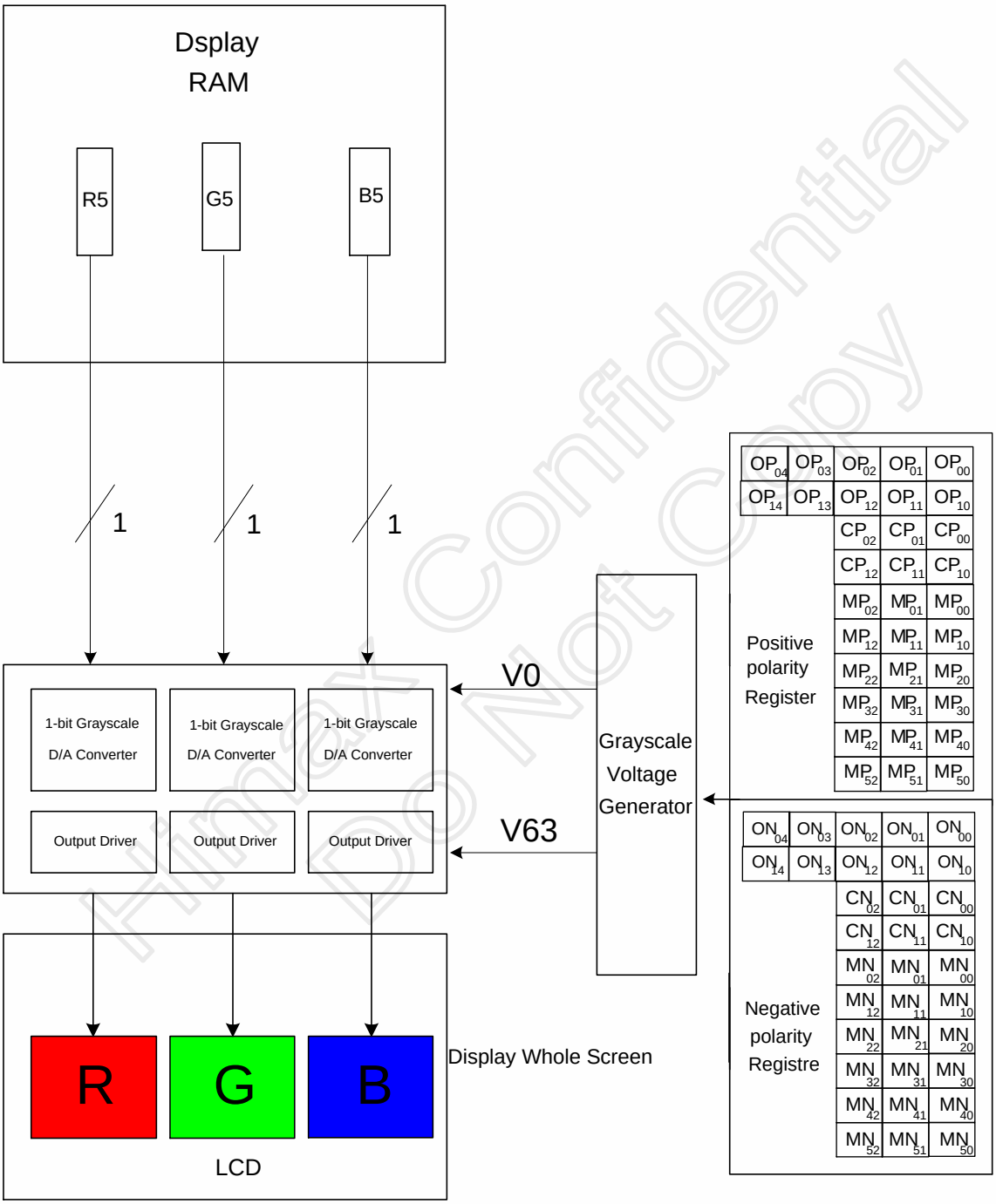


Figure 9. 1 Grayscale Control in 8-Color Display Mode

10. Display Operation Control

10.1 Display Driving Period Time Control

The HX8312-A can control the display operation period time for LCD panel driving as follow:

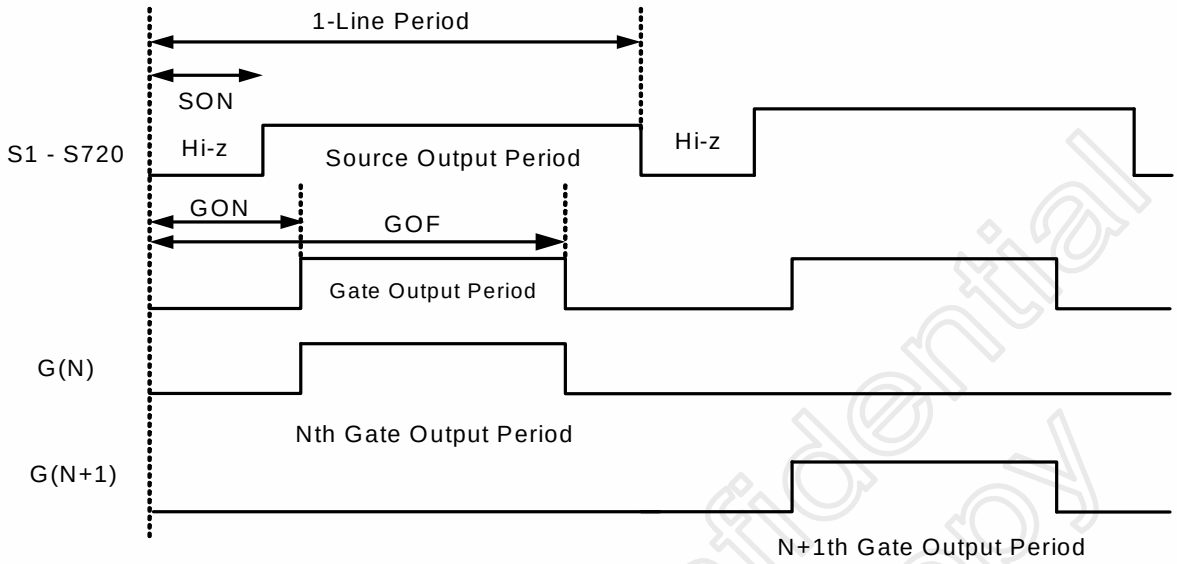


Figure 10. 1 Display Driving Period Time Setting

D7	D6	D5	D4	D3	D2	D1	D0
SON7	SON6	SON5	SON4	SON3	SON2	SON1	SON0

Table 10. 1 Source on register (R136)

SON7-0: Specify the valid source output start time in 1-line driving period. The period time is defined as SYSCLK clock number.

Please note that the setting “00h” and “01h” is inhibited**.**

D7	D6	D5	D4	D3	D2	D1	D0
GON7	GON6	GON5	GON4	GON3	GON2	GON1	GON0

Table 10. 2 Gate on register (R137)

SON7-0: Specify the valid gate output start time in 1-line driving period.
The period time is defined as SYSCLK clock number in internal clock display mode.
The period time is defined as setting value x 8 DOTCLK clock number in external clock display mode.

Please note that the setting “00h” ,“01h”, “02h” is inhibited**.**

Gate off register 1 (R134)

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	-	-	GOF8

Gate off register 2 (R135)

D7	D6	D5	D4	D3	D2	D1	D0
GOF7	GOF6	GOF5	GOF4	GOF3	GOF2	GOF1	GOF0

Table 10. 3 Gate off register

GOF8-0: Specify the gate output end time in 1-line driving period.
The period time is defined as SYSCLK clock number in internal clock display mode.
The period time is defined as setting value x 8 DOTCLK clock number in external clock display mode.

Please note that the GOF8-0 ≤ HCK-1

10.2 All "0" or "1" Source Output Display

By setting DISP1 and DISP0 (D7-6 bits of R0), HX8312-A can display data "0" or "1" on the whole LCD regardless of display RAM data and the data in the display RAM is not changed.

D7	D6	D5	D4	D3	D2	D1	D0
DISP1	DISP0	ADC	DTY	STBY	COLOR	-	GSM

Table 10. 4 Control register 1 (R0)

DISP1-0:

DISP1	DISP0	Display
0	0	Output display data from display RAM
0	1	All Output "0" regardless of the display data in display RAM
1	0	All output "1" regardless of the display data in display RAM
1	1	All output "1" regardless of the display data in display RAM

10.3 Gate Scanning Stop Control

Gate scanning can be stopped by setting DISPTMG (D0 bit of R59) as "0" All gate scans will be stopped if DISPTMG = "0", however, the frame frequency doesn't change.
GOE 1 output control register (R59)

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	-	-	DISPTMG

Table 10. 5 Gate output control register (R59)

11. Scan Mode Setting

11.1 Scan Pattern

The number of gate-drive lines can be set by NSO1-0 (D2-1 bits of R13). Refer to "4.1 Relation between Display Data RAM and the LCD Panel".

The HX8312-A can set R/L (D3 bit of R29) and SCN[2:0] (D2-0 bits of R29) bits to determine the shift direction of gate outputs for different panel layout. And the DDS pin is used to set the position of dummy output pin in each mode. (Refer to "11.2. Blanking Period and Dummy Line Location")

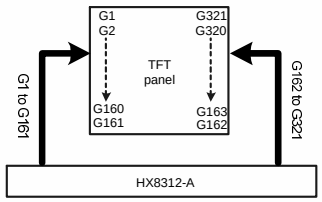
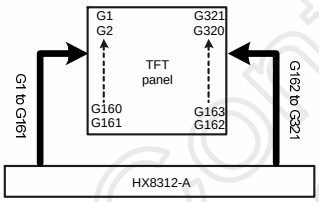
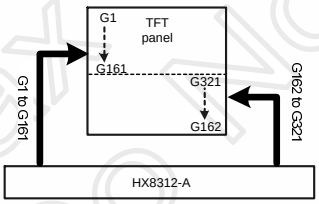
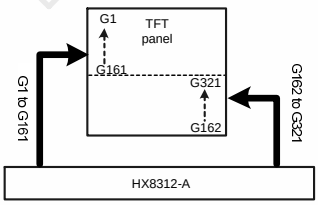
R/L	SCN[2:0]	Scan direction	DDS pin	
1	XX 0	 MODE5R mode	0	G1, G321, G2, G320, ... , G159, G163, G160, G162, (G161 dummy)
			1	(G1 dummy), G321, G2, G320, ... , G159, G163, G160, G162, G161
0	XX 0	 MODE5R mode	0	G161, G162, G160, G163, ... , G3, G320, G2, G321, (G1 dummy)
			1	(G161 dummy), G162, G160, G163, ... ,G3, G320, G2, G321, G1
1	01 1	 MODE2R mode	0	G1, G2, ... , G160, G161, G321, G320, G319, ... , G163, (G162 dummy)
			1	(G1 dummy), G2, ... , G160, G161, G321, G320, ... , G163, G162
0	01 1	 MODE2L mode	0	G162, G163, G164, ... , G320, G321, G161, G160, ... , G3, G2, (G1 dummy)
			1	(G162 dummy), G163, G164, ..., G321, G161, G160, ... , G3, G2, G1

Figure 11. 1 SCAN Mode Setting

Scan pattern mode	R/L R29:D3	SCN2 R29:D2	SCN1 R29:D1	SCN0 R29:D0	DDS pin	Dummy pin	Scan Order
MODE5R	1	X	X	0	0	G161	G1, G321, G2, G320, …, G159, G163, G160, G162, (dummy)
					1	G1	(dummy), G321, G2, G320, …, G159, G163, G160, G162, G161
MODE5L	0	X	X	0	0	G1	G161, G162, G160, G163, …, G3, G320, G2, G321, (dummy)
					1	G161	(dummy), G162, G160, G163, …, G3, G320, G2, G321, G1
MODE2R	1	0	1	1	0	G162	G1, G2, …, G160, G161, G321, G320, G319, …, G163, (dummy)
					1	G1	(dummy), G2, …, G160, G161, G321, G320, …, G163, G162
MODE2L	0	0	1	1	0	G1	G162, G163, G164, …, G320, G321, G161, G160, …, G3, G2, (dummy)
					1	G162	(dummy), G163, G164, …, G321, G161, G160, …, G3, G2, G1

Table 11. 1 Scan Mode Setting

11.2 Blanking Period and Dummy Line Location

The dummy line number selection register (R118) is used for setting the blanking period between two frame scan. The external DDS pin of HX8312-A determines to put the blanking period and a dummy line whether at the head or the end of a frame.

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	-	-	DMYSEL

Table 11. 2 Dummy line number selection register (R118)

DMYSEL: sets dummy line number of the blanking period
"0": one dummy line scan
"1": one dummy line scan + 7-line blanking period
(In blanking period, LC AC alternated source drive and the gate output OFF)

DDS pin	Blanking Period Location
0	End: 1 frame scan + dummy (+7 blanking)
1	Head: (7 blanking +) dummy + 1 frame scan

Table 11. 3 DDS pin set-up

Note:1.Please set R118:D0=DMYSEL as "0" when 3-field interlaced driving mode is selected.
(DMYSEL="1" is not available when Skip 2B is selected)
2. R118 is not valid when the LCD displays operation is in synchronization with an external clock

12. Oscillation Circuit

The HX8312-A can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor (Rf) or internal oscillation resistor 100Kohm(select by ROSC setting, D0 bit of R43). The oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If Rf is increased or power supply voltage is decreased, the oscillation frequency decreases.

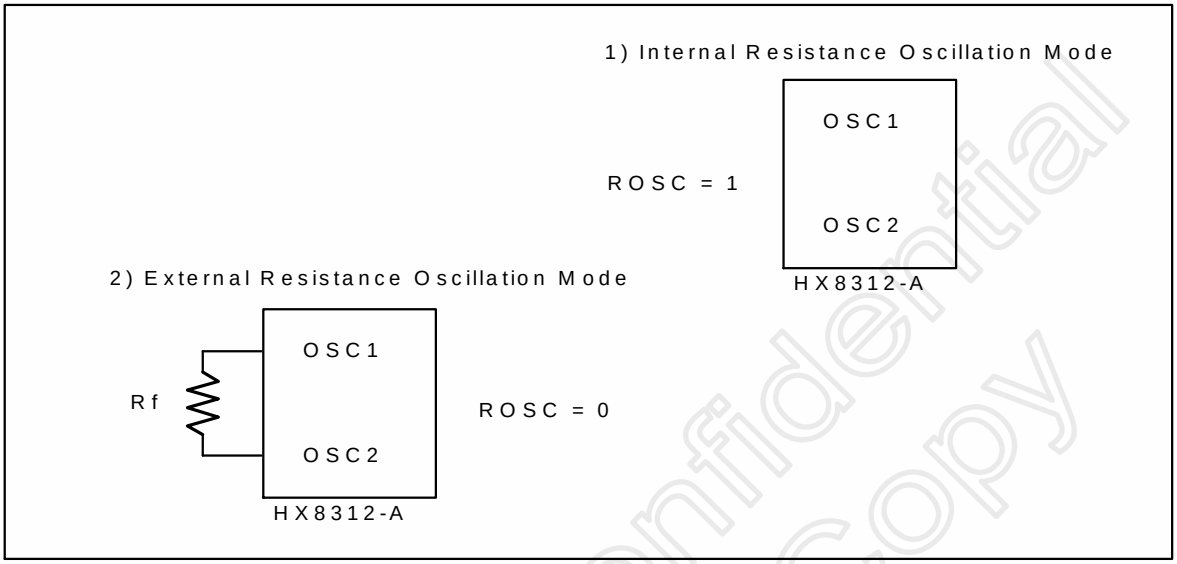


Figure 12. 1 Oscillation Circuit

The oscillation frequency can be adjust finely by setting RADJ2-0 (D3-1 bits of R43) as follow:

Internal R: 100 K ohm		RC oscillation frequency (MHz)		
RADJ[2:0]	correction	Vcc=2.5V	Vcc=2.8V	Vcc=3.3V
000	No	1.561	1.820	2.215
001	-10%	1.434	1.640	1.953
010	-20%	1.313	1.480	1.718
011	-30%	1.181	1.310	1.495
100	+10%	1.677	1.990	2.444
101	+20%	1.788	2.153	2.688
110	+30%	1.898	2.305	2.943
111	+40%	2.023	2.482	3.25

Table 12. 1 Frequency Adjustment (ROSC = 1)

The oscillation circuit on / off control can be defined by the OSCSTBY setting (D0 bit of R1), When OSCSTBY = “0”, the oscillation circuit start to oscillate; when OSCSTBY = “1”, the oscillation circuit stop to oscillate.

13. Power Generation

13.1 Power Supply Set up

HX8312-A has an internal power supply circuit to drive TFT LCD panel. Please set up each voltage output according to the LCD panel.

Name	Function	Set up Value	Note
VR1	Reference voltage for VR2 / DDVDH / VS / VDH generation	Vci x A (*1)	VR1 ≤ Vci – 0.15
VR2	Reference voltage for VGH generation	VR1 x B (*2)	VR2 ≤ Vci – 0.15
DDVDH	Step-up circuit 1 output Power supply for VS/VR/VDH/VCOM	VR1 x 2	Do not exceed 5.5V
VGH	(Step-up circuit 2 output) Gate on voltage	VR1 x C (*3)	Do not exceed 16.5V
VGL	(Step-up circuit 2 output) Gate off voltage	VR2 x D - VR1 x E (*3)	Do not lower than –16.5V
VCL	(Step-up circuit 3 output) Power supply for VCOML generation	Vci x (-1)	-
VS	Power supply for the source circuit output driving	VR1 x F (*4)	3.5V – 5.25V
VDH	Reference voltage for gamma circuit	VR1 x F (*4)	
VCOMH	VCOM high voltage	VS x G (*5)	-
VCOML	VCOM low voltage	VCOMH – VSxH (*6)	-
VCOM	VCOM voltage	-	Output VCOMH and VCOML voltage alternately.
V18	Logic power supply	1.8V	-

Table 13. 1 Power Supply Voltage Configuration

Note : 1. The value of A is determined by VR1SEL2-0 bits (D4-2 bits of register R25).
2. The value of B is determined by VR2SEL2-0 bits (D7-5 bits of register R25).
3. The value of C , D and E is determined by BT3-0 bits (D3-0 bits of register R37) setting and C21+ , C21- pin connection.
4. The value of F is determined by VSEL2-0 bits (D3-1 bits of register R27).
5. The value of F is determined by VCM4-0 bits (D4-0 bits of register R32).
6. The value of G is determined by VDV4-0 bits (D4-0 bits of register R31).

The voltage setting diagram of power output for LCD panel driving setup diagram is as follow:

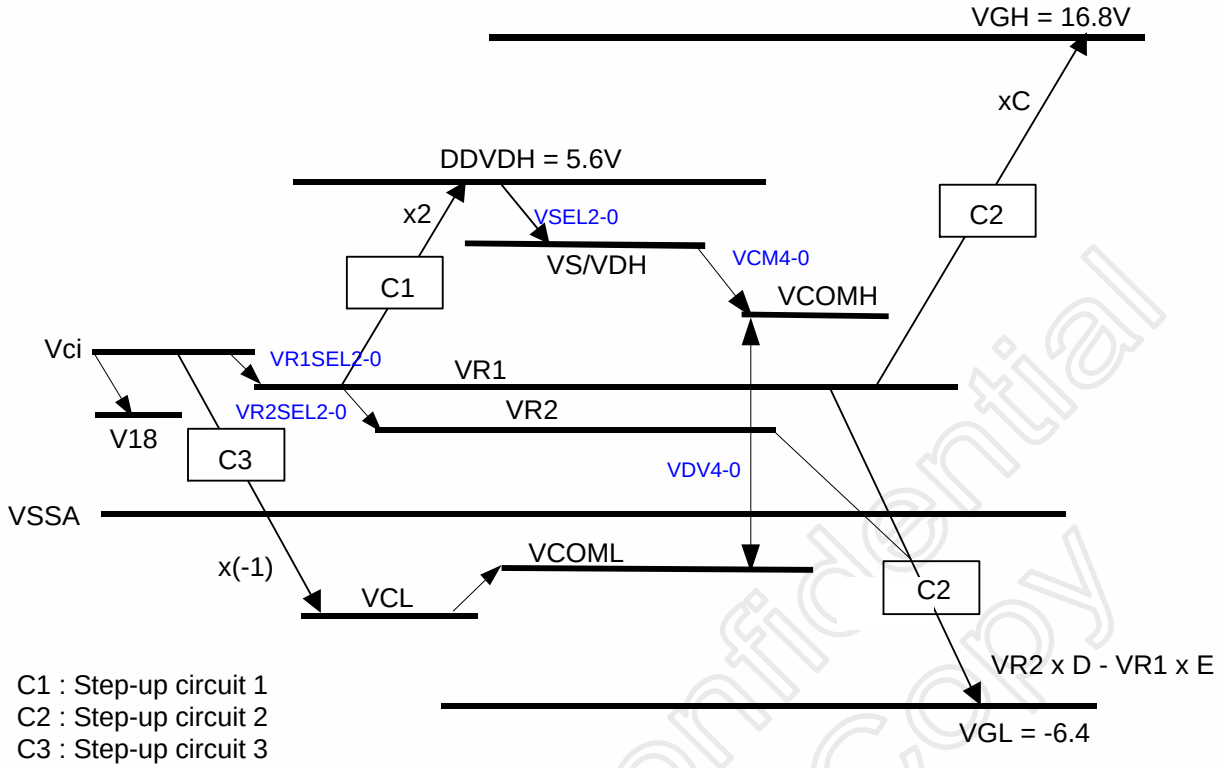


Figure 13. 1 Voltage setting diagram

13.2 Power Supply Register

The on/off control of each power output is defined by power supply system control register 1 (R24)

D7	D6	D5	D4	D3	D2	D1	D0
VR2ON	VR1ON	VCLON	VGON	-	DDVDHON	-	DCON

Table 13. 2 Power supply system control register 1 (R24)

VR2ON: VR2 regulator output control.
"0": VR2 regulator off, VR2 output = Hi-z.
"1": VR2 regulator on.

VR1ON: VR1 regulator output control.
"0": VR regulator off, VR2 output = VSSA.
"1": VR1 regulator on.

VCLON: Step up circuit 3 output control

Register			Step up Circuit	Output
DCON (D0 bit of R24)	STBY (D3 bit of R0)	VS4ON (D5 bit of R24)	C3	VCL
0	X	X	Stop	VSSA
1	1	X	Stop	VSSA
1	0	0	Stop	VSSA
1	0	1	ON	Active

VGON: Step up circuit 2 output control

Register			Step up Circuit	Output	
DCON (D0 bit of R24)	STBY (D3 bit of R0)	VGON (D4 bit of R24)	C2	VGH	VGL
0	X	X	Stop	DDVDH	VSSA
1	1	X	Stop	DDVDH	VSSA
1	0	0	Stop	DDVDH	VSSA
1	0	1	ON	Active	Active

DDVDHON: Step up circuit 1 output control

Register			Step up Circuit	Output
DCON (D0 bit of R24)	STBY (D3 bit of R0)	DDVDHON (D2 bit of R24)	C1	DDVDH
0	X	X	Stop	VR1
1	1	X	Stop	VR1
1	0	0	Stop	VR1
1	0	1	ON	Active

VDCON: DC/DC Converter output control
"0": DC/DC Converter off.
"1": DC/DC Converter on.

D7	D6	D5	D4	D3	D2	D1	D0
VR2SEL2	VR2SEL1	VR2SEL0	VR1SEL2	VR1SEL1	VR1SEL0	-	-

Table 13. 3 Power supply system control register 2 (R25)

VR2SEL2-0 specify the output voltage of the VR2regulator. (VR2 ≤ Vci – 0.15V)

VR2SEL2	VR2SEL1	VR2SEL0	VR2
0	0	0	VR1
0	0	1	VR1 x 0.9
0	1	0	VR1 x 0.8
0	1	1	VR1 x 0.7
1	0	0	VR1 x 0.6
1	0	1	VR1 x 0.5
1	1	0	Hi-Z
1	1	1	Hi-Z

VR1SEL2-0 specify the output voltage of the VR1regulator. (VR1 ≤ Vci – 0.15V)

VR1SEL2	VR1SEL1	VR1SEL0	VR1
0	0	0	Vci
0	0	1	Vci x 0.93
0	1	0	Vci x 0.88
0	1	1	Vci x 0.82
1	0	0	Vci x 0.78
1	0	1	Vci x 0.74
1	1	0	Setting Disable
1	1	1	Setting Disable

D7	D6	D5	D4	D3	D2	D1	D0
DCCLK7	DCCLK6	DCCLK5	DCCLK4	DCCLK3	DCCLK2	DCCLK1	DCCLK0

Table 13. 4 Power supply system control register 3 (R40)

DCCLK7-0 : specify the clock frequency for DC/DC converter operating.

DCCLK7	DCCKL6	DCCLK5	DCCLK4	DCCLK3	DCCLK2	DCCLK1	DCCLK0	DCDCf
0	0	0	0	0	0	0	0	Inhibited
0	0	0	0	0	0	0	1	SYSCLK
0	0	0	0	0	0	1	0	SYSCLK / 2
1	1	1	1	1	1	1	0	SYSCLK / 254
1	1	1	1	1	1	1	1	SYSCLK / 255

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	DC3	DC2	DC1	DC0

Table 13. 5 Power supply system control register 3 (R26)

DC3-2 : specify the operating frequency for step up circuit 2 and 3

DC3	DC2	Frequency for step up 2 and 3
0	0	DCDCf / 1
0	1	DCDCf / 2
1	0	DCDCf / 4
1	1	DCDCf / 8

DC1-0 : specify the operating frequency for step up circuit 1

DC1	DC0	Frequency for step up 1
0	0	DCDCf / 1
0	1	DCDCf / 2
1	0	DCDCf / 4
1	1	DCDCf / 8

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	VSEL2	VSEL1	VSEL0	RGON

Table 13. 6 Power supply system control register 4 (R27)

VSEL2-0 specify the output voltage of the VS and VDH regulator.

VSEL2	VSEL1	VSEL0	VS / VDH
0	0	0	VR1 x 1.38
0	0	1	VR1 x 1.45
0	1	0	VR1 x 1.53
0	1	1	VR1 x 1.6
1	0	0	VR1 x 1.68
1	0	1	VR1 x 1.75
1	1	0	VR1 x 1.83
1	1	1	Setting Disable

Note: Make sure VS / VDH ≤ DDVDH –0.15.

RGON control the output on/off of the VS and VDH regulator.
"0": Off, The VS output is Hi-Z and the VDH output is VSSA.
"1": On.

D7	D6	D5	D4	D3	D2	D1	D0
VCOMEN	-	VCOMFX	VCOMHI	XVCOMG	-	-	DDVDHXON

Table 13. 7 Power supply system control register 8 (R30)

VCOMEN, VCOMFX, VCOMHI specify the VCOM circuit operation.

VCOMEN	VCOMFX	VCOMHI	VCOM Circuit	VCOM Output
0	X	X	Stand-by	VSSA
1	X	1	Operation	Hi-Z
1	1	0	Operation	VSSA
1	0	0	Operation	Normal Operation

DDVDHXON specify whether or not to use an extra step-up circuit capacitor CX11 for stronger DDVDH generation.
"0" : Doesn't use the extra step-up circuit CX11.
"1" : Use the extra step-up circuit C!x.

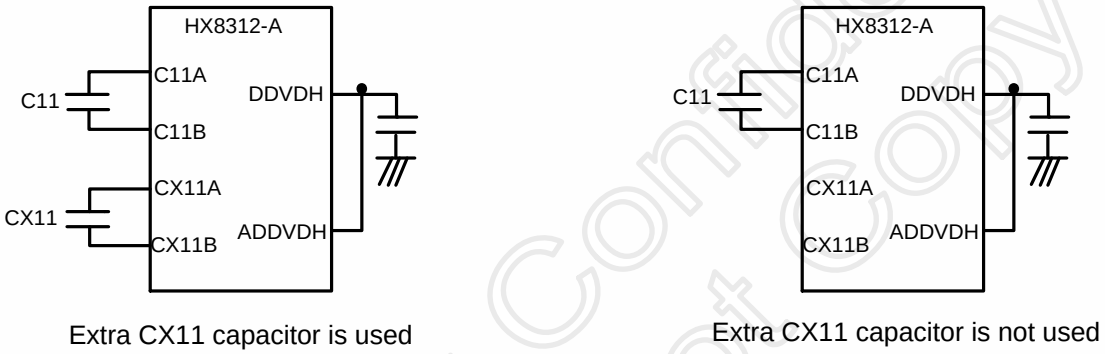


Figure 13. 2 Configuration of the Step up Circuit 1

XVCOMG specify VCOML output level.
"0" : Specified by register R31 and R32.
"1" : VSSA.

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	VDV4	VDV3	VDV2	VDV1	VDV0

Table 13. 8 Power supply system control register 9 (R31)

VDV4-0 specify the amplitude of VCOM output alternating voltage.

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM Amplitude
0	0	0	0	0	VS x 0.60
0	0	0	0	1	VS x 0.63
0	0	0	1	0	VS x 0.66
			•		
			•		
0	1	1	0	1	VS x 0.99
0	1	1	1	0	VS x 0.102
0	1	1	1	1	Setting Disable
1	0	0	0	0	VS x 1.05
1	0	0	0	1	VS x 1.08
1	0	0	1	0	VS x 1.11
1	0	0	1	1	VS x 1.14
1	0	1	0	0	VS x 1.17
1	0	1	0	1	VS x 1.20
1	0	1	1	0	VS x 1.23
1	0	1	1	1	Setting Disable
1	1	x	x	x	Setting Disable

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	VCM4	VCM3	VCM2	VCM1	VCM0

Table 13. 9 Power supply system control register 9 (R31)

VCM4-0 specify the high level of VCOM output alternating voltage (VCOMH).

VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	VS x 0.40
0	0	0	0	1	VS x 0.42
0	0	0	1	0	VS x 0.44
				•	
				•	
0	1	1	0	1	VS x 0.66
0	1	1	1	0	VS x 0.68
0	1	1	1	1	Internal adjustment halt VCOMH = External pin VcomR input.
1	0	0	0	0	VS x 0.70
1	0	0	1	0	VS x 0.72
1	0	0	1	1	VS x 0.74
				•	
				•	
1	1	1	0	0	VS x 0.94
1	1	1	0	1	VS x 0.96
1	1	1	1	0	VS x 0.98
1	1	1	1	1	Internal adjustment halt VCOMH = External pin VcomR input.

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	BT3	BT2	BT1	BT0

Table 13. 10 Power supply system control register 12 (R37)

BT2-0 specify the DDVDH, VGH and VGL output voltage level.

C21 capacitor is used

BT3	BT2	BT1	BT0	VGH	VGL
0	0	0	0	VR1 x 8	-VR1 x 7
0	0	0	1	VR1 x 8	-VR1 x 6
0	0	1	0	VR1 x 8	VR2- VR1 x 6
0	0	1	1	VR1 x 7	-VR1 x 7
0	1	0	0	VR1 x 7	-VR1 x 6
0	1	0	1	VR1 x 7	VR2- VR1 x 6
0	1	1	0	VR1 x 6	-VR1 x 6
0	1	1	1	VR1 x 6	VR2- VR1 x 6
1	0	0	0	VR1 x 6	-VR1 x 4
1	0	0	1	VR1 x 6	VR2- VR1 x 4
1	0	1	0	VR1 x 6	-VR1 x 3
1	0	1	1	VR1 x 6	VR2- VR1 x 3
1	1	0	0	VR1 x 5	-VR1 x 5
1	1	0	1	VR1 x 5	-VR1 x 4
1	1	1	0	VR1 x 5	-VR1 x 3
1	1	1	1	VR1 x 5	VR2- VR1 x 3

C21 capacitor is not used

BT3	BT2	BT1	BT0	VGH	VGL
0	0	0	0	VR1 x 6	-VR1 x 5
0	0	0	1	VR1 x 6	-VR1 x 4
0	0	1	0	VR1 x 6	VR2- VR1 x 4
0	0	1	1	VR1 x 5	-VR1 x 5
0	1	0	0	VR1 x 5	-VR1 x 4
0	1	0	1	VR1 x 5	VR2- VR1 x 4
0	1	1	0	VR1 x 4	-VR1 x 4
0	1	1	1	VR1 x 4	VR2- VR1 x 4
1	0	0	0	VR1 x 4	-VR1 x 2
1	0	0	1	VR1 x 4	VR2- VR1 x 2
1	0	1	0	VR1 x 4	-VR1 x 1
1	0	1	1	Inhibit	
1	1	0	0	VR1 x 3	-VR1 x 3
1	1	0	1	VR1 x 3	-VR1 x 2
1	1	1	0	VR1 x 3	-VR1 x 1
1	1	1	1	Inhibit	

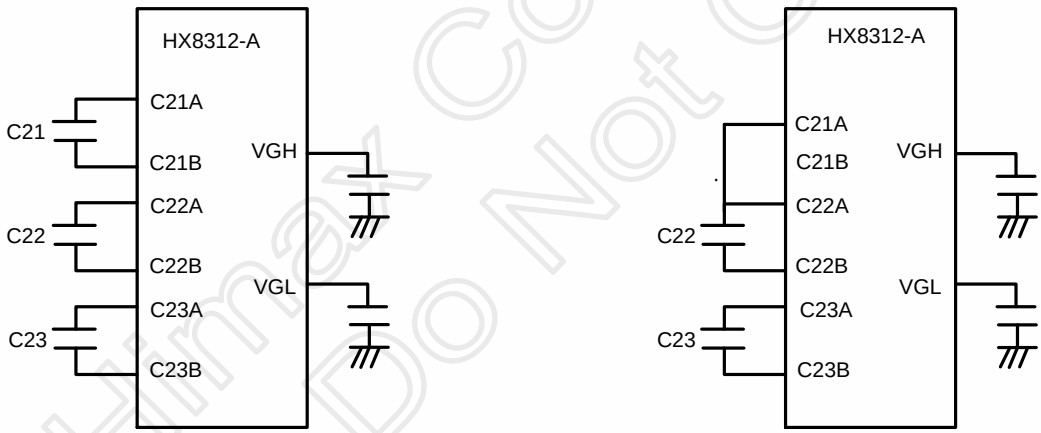


Figure 13. 3 Configuration of the Step up Circuit 2

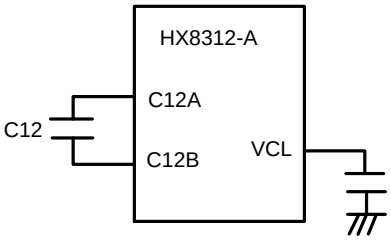


Figure 13. 4Configuration of the Step up Circuit 3

14. Set up Sequence

14.1 On / Off Sequence

Register	Setting Value	D7	D6	D5	D4	D3	D2	D1	D0	Operation
VCC, VCI, IOVCC On										
R1	“xx” h	x	x	0	0	0	0	x	0	Start oscillation.
R0	“xx” h	x	x	x	x	0	x	0	x	Stand by mode cancel.
R3	“01” h	0	0	0	0	0	0	0	1	Software reset operation.
Wait for 10ms										
R3	“00” h	0	0	0	0	0	0	0	0	Software reset cancel.
R43	“0x” h	0	0	0	0	x	x	x	x	Oscillation frequency adjust.
R40	“xx” h	x	x	x	x	x	x	x	x	DCDCf setting.
R26	“0x” h	0	0	0	0	x	x	x	x	Step up circuit frequency setting.
R37	“0x” h	0	0	0	0	x	x	x	x	Step up circuit 2 factor setting.
R28	“3x” h	0	0	1	1	0	x	x	x	Set the step-up circuit operating current.
R30	“0x” h	0	0	0	0	x	0	0	1	Set extra CP1 available.
R25	“xx” h	x	x	x	x	x	x	0	0	Set the VR1, VR2 regulator to fit to LCD module.
R24	“C1” h	1	1	0	0	0	0	0	1	Set VR1 and VR2 regulator on.
Wait for 10ms										
R24	“E1” h	1	1	1	0	0	0	0	1	VCL turn on.
R24	“F1” h	1	1	1	1	0	1	0	1	VGH / VGL turn on.
Wait for 60ms										
R24	“F5” h	1	1	1	1	0	1	0	1	DDVDH turn on.
Wait for 60ms										
R27	“0x” h	0	0	0	0	x	x	x	1	VS / VDH set and VS / VDH turn on.
Wait for 10ms										
R32	“xx” h	0	0	0	x	x	x	x	x	Set VCOMH voltage.
R31	“xx” h	0	0	0	x	x	x	x	x	Set VCOM amplitude.
R30	“8x” h	1	0	0	0	x	0	0	1	VCOM start
Wait for 10ms										

Table 14. 1 Power On Sequence

Note : “x“ means that set the value to meet LCD module characteristic.

Register	Setting Value	D7	D6	D5	D4	D3	D2	D1	D0	Operation
R30	“0x” h	0	0	0	0	x	0	0	1	VCOM stop
R27	“0x” h	0	0	0	0	x	x	x	0	VS / VDH turn off.
R24	“C0” h	1	1	0	0	0	0	0	0	CP1, CP2, CP3 turn off.
Wait for 10ms										
R24	“00” h	0	0	0	0	0	0	0	0	VR1 / VR2 Off.
R28	“30” h	0	0	1	1	0	0	0	0	Step up circuit operating current stop.
VCC, VCI, IOVCC Off										

Table 14. 2 Power Off Sequence

Register	Setting Value	D7	D6	D5	D4	D3	D2	D1	D0	Operation
R0	“xx” h	1	0	x	x	0	x	0	x	White display mode setting.
R59	“01” h	0	0	0	0	0	0	0	1	Gate scan start.
Wait for 2 frame scan										
R0	“xx” h	0	0	x	x	0	x	0	x	Normal display operation start.

Table 14. 3 Display On Sequence

Register	Setting Value	D7	D6	D5	D4	D3	D2	D1	D0	Operation
R0	“xx” h	1	0	x	x	0	x	0	x	White display mode setting.
Wait for 2 frame scan										
R59	“00” h	0	0	0	0	0	0	0	0	Gate scan stop.

Table 14. 4 Display Off Sequence

14.2 Operation Sequence

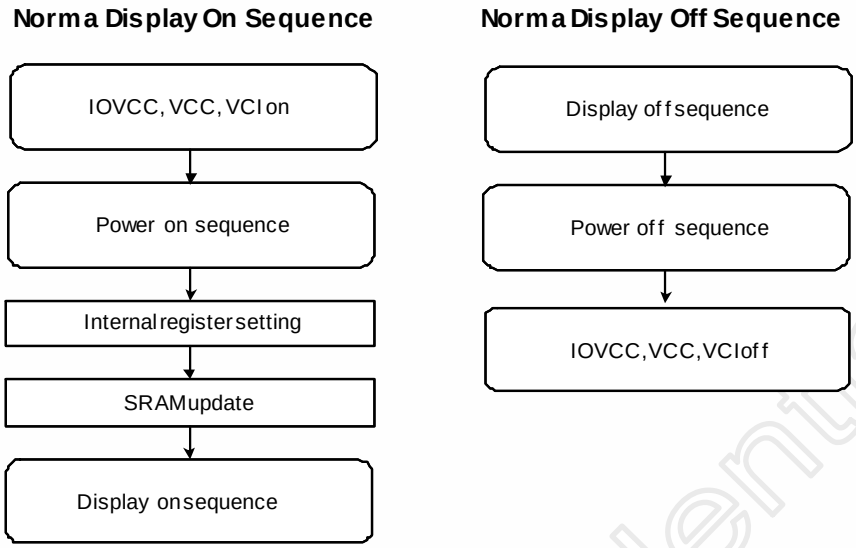
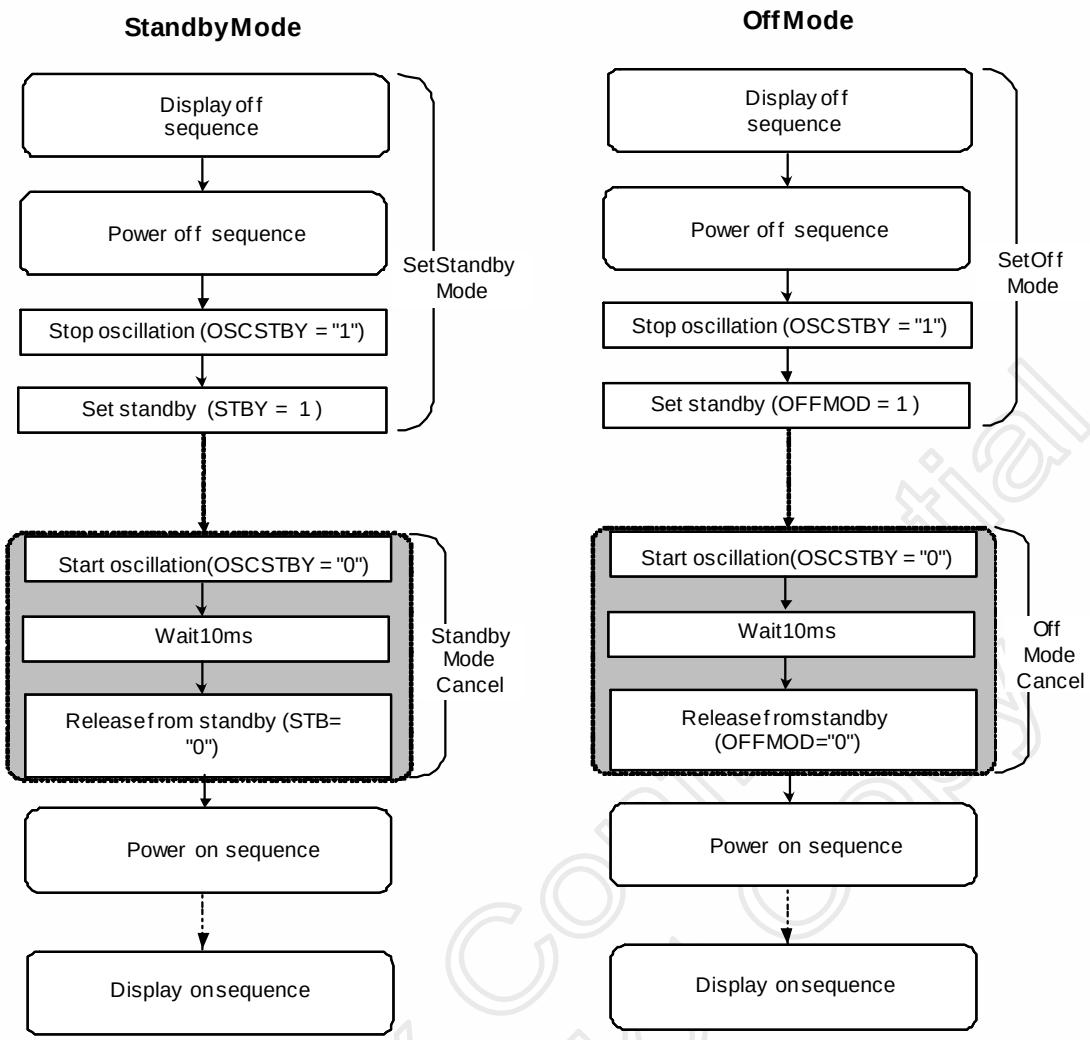


Figure 14. 1 Normal Display On / Off Sequence



Note : In off mode, only OFFMOD bit (D7 bit of R192) can be updated. Other register and the display RAM can not be updated. The display RAM data may not be retained in off mode, and need to rewrite after off mode canceling.

Figure 14. 2 Standby Mode and OFF Mode Sequence

15. System Configuration

15.1 System Diagram

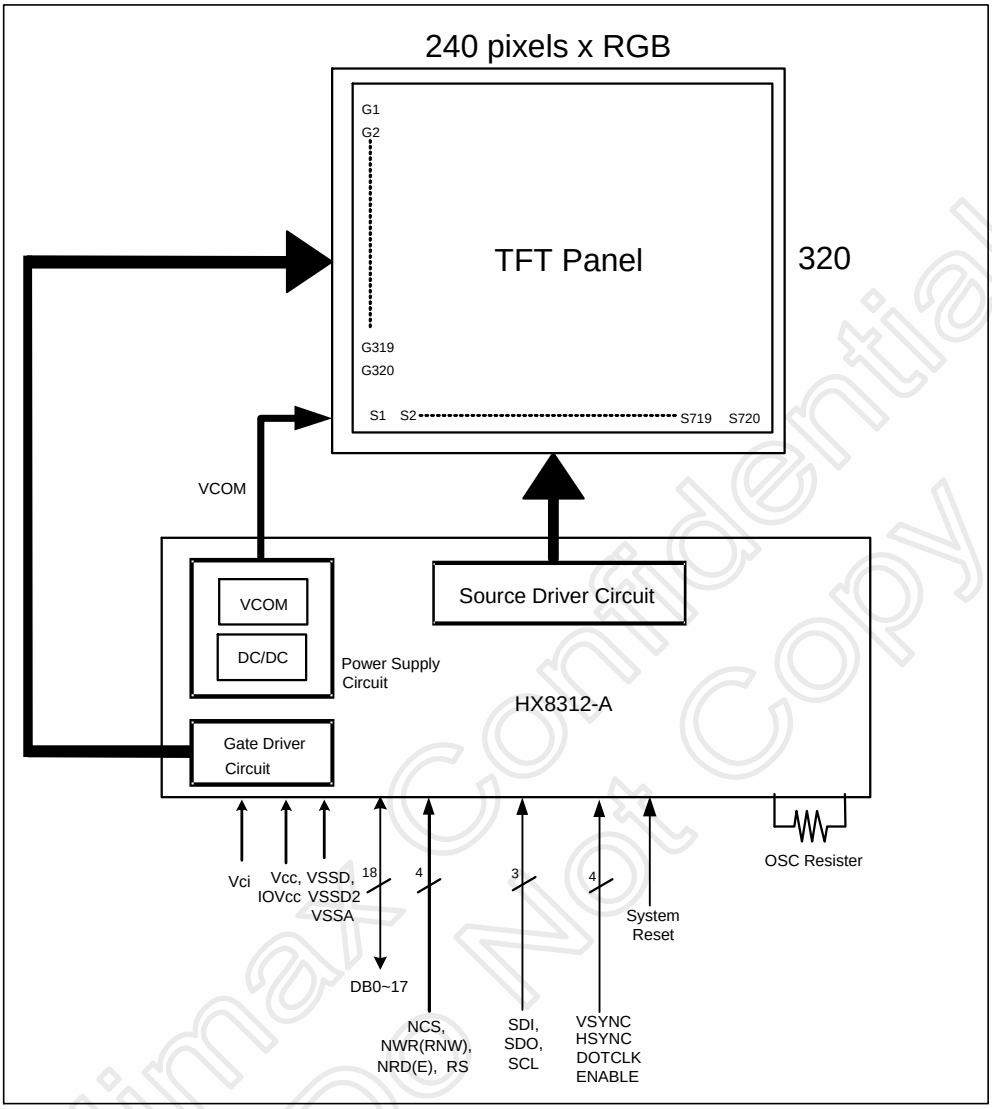


Figure15. 1 System Diagram of HX8312-A

15.2 Layout Recommendation

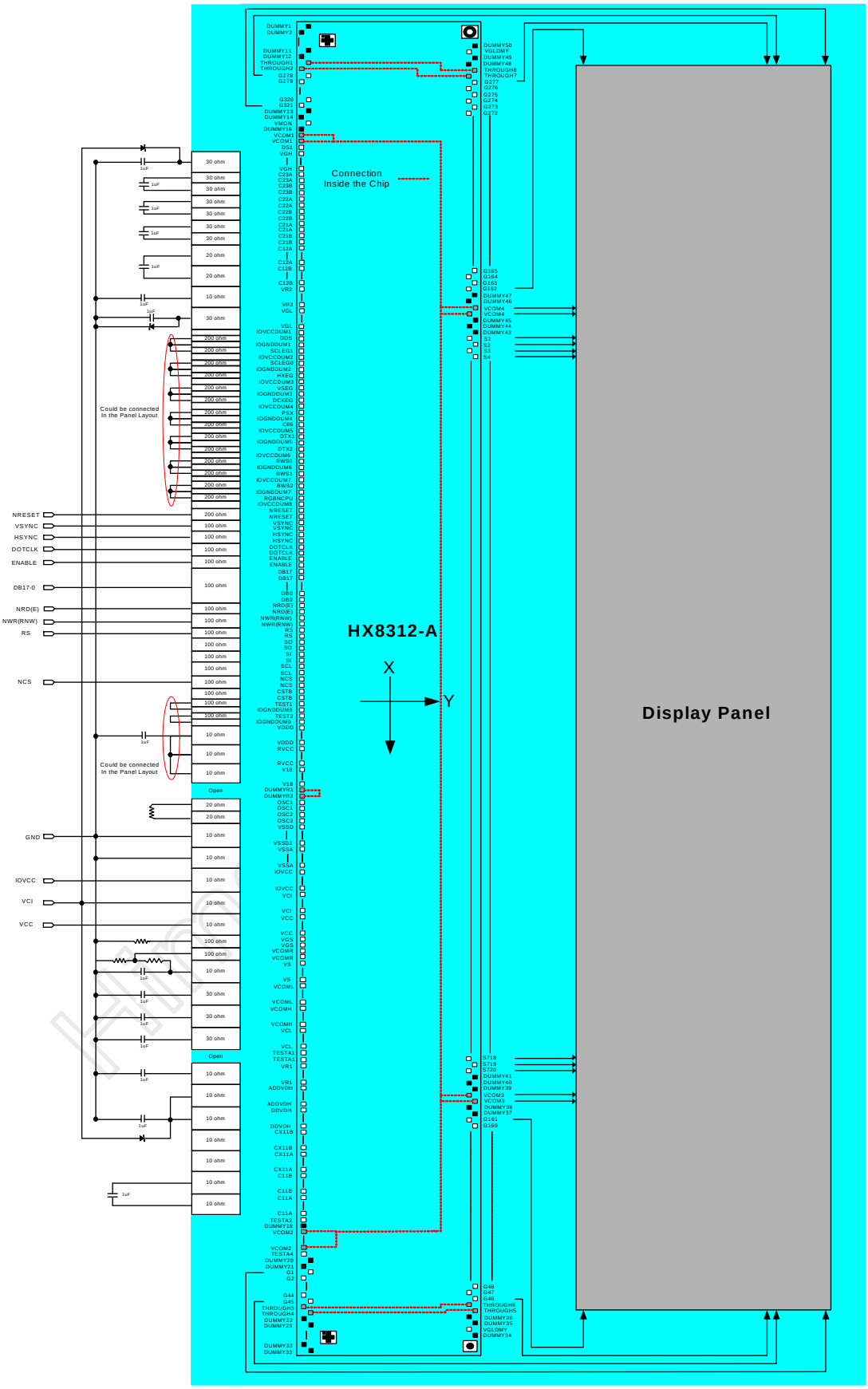


Figure15. 2 Layout Recommendation of HX8312-A

15.3 Recommended Passive Components for the Step-up circuits and Others

The specification of recommended passive components used for the step up circuits and others are listed as following table.

Pins connection	Recommended voltage	Capacity
VDDD	6V	1 µF (B characteristics)
C11A/B, CX11A/B, C12A/B, VCL, VR1, VR2, VS, VCOMH, VCOML, DDVDH	10V	1 µF (B characteristics)
C21A/B, C22A/B, C23A/B, VGH, VGL	25V	1 µF (B characteristics)

Table 15. 1 The adoptability of Capacitor

Pins connection	Feature
(VSSA – VGL) (VCI – VGH) (VCI – DDVDH)	VF < 0.4V / 20mA at 25°C, VR ≥30V

Table 15. 2 The adoptability of Schottkey diode

Pins connection	Feature
VcomR	> 200 kΩ

Table 15. 3 The adoptability of Variable resistor

16. Register Description

Register	Bit	Symbol	Function	Configuration
R0 (R00h) default “A0“h	Control register 1			
	D7	DISP1	Source output data selection.	All source output as “0” or “1” selection Refer to "10.2 “ All "0" or "1" Source Output Display “
	D6	DISP0	Source output data selection.	All source output as “0” or “1” selection Refer to "10.2 “ All "0" or "1" Source Output Display “
	D5	ADC	Specifies source output and display RAM address mapping.	Refer to 4.1 “Relation between the Display RAM Address and the Source Output Channel”
	D4	DTY	Specifies partial display mode.	"0" : Normal display mode. "1" : Partial display mode. Refer to "5. Partial Display Mode".
	D3	STBY	Specifies stand-by mode.	"0" : Normal operation. "1" : Stand-by mode.
	D2	COLOR	Specifies color mode.	"0" : 262,144 color mode. "1" : 8 color mode. Refer to "9 8-color Display Mode".
	D1	-	-	-
	D0	GSM	Gate scan selection in partial-off display areas.	"0" : Normal scan in non-display area "1" : Configures the scanning cycle in non-display area by the number of the R52 register.
R1 (R01h) default “00“h	Control register 2			
	D7	ADX	RAM X address increment direction after one write or read operation .	"0" : From X0 to X239 Refer to "4.2. Display RAM Access” ”1” : From X239 to X0 *Note : ADX = “1” setting is prohibited when RGB interface circuit is in use.
	D6	ADR	RAM Y address increment direction after one write or read operation .	“0” : Y0 to Y319 Refer to "4.2. Display RAM Access” ”1” : Y319 to Y0 *Note : ADR = “1” setting is prohibited when RGB interface circuit is in use.
	D5	-	-	-
	D4	GSEL	Specifies voltage level of V0 and V63	“0” : V0=VDH, V63 = VSSA. “1” : Depends on the OP0/1 and CP0/1 register setting. Refer to “8 Gamma Adjustment Function”.
	D3	-	-	-
	D2	-	-	-
	D1	LTS	Specifies setting period of calibration.	“0” : 1line period = tcal ”1” : 1 line period = tcal x 2 Refer to "3.3 Internal Clock Mode".
	D0	OSCSTBY	Oscillation control.	“0” : Starts oscillation. ”1” : Stops oscillation.
RGB interface register 2				
R2 (R02h) default “00“h	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	VMODE	VSYNC interface selection.	“0” : Normal Refer to "Table 9. 1". “1” : Uses VSYNC interface.
	D3	-	-	-
	D2	RGBS	RGB interface writing mode selection.	“0” : Capture mode. Refer to "Table 9. 1". ”1” : Through mode.
	D1	DISPCK	Specifies display timing at RGB interface circuit.	“0” : Internally synchronized display mode by SYSCLK. ”1” : Externally synchronized display mode by VSYNC and HSYNC. Refer to "Table 9. 1".
	D0	NWRGB	RGB interface pin control.	“0” : Writes to the display data RAM via the system interface circuit. ”1” : Writes to the display data RAM via the RGB interface circuit. Refer to "Table 9. 1".

R3 (R03h) default “00“h	**Reset register 1**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	RES	Reset command for the HX8312-A	"0" : Normal operation. "1" : Reset Operation.
R5 (R05h) default “00“h	**RAM access control register**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	WAS	Specifies window area access mode.	"0" : Normal writing mode. "1" : Window area access mode. Refer to "4.3. Window Area Access Mode".
	D3	-		
	D2	AM	Specifies the address increment direction.	"0" : X address increment, then Y address increment. "1" : Y address increment, then X address increment, *Note: This setting is invalid when RGB interface circuit is in use. Refer to "4.2. Access to the Display Data RAM".
	D1	-	-	-
	D0	-	-	-
R6 (R06h) default “00“h	**Data reverse register**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	REV	Reverse the source output data voltage	“0”: Data “0000”h; Source output: V0 at VCOML “1”: Data “0000”h; Source output V63 at VCOML
R13 (R0Dh) default “00“h	**Display size control register**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	NSO1	Specify source output size.	Refer to "4.1 Relation between the Display RAM Address and the Source Output Channel”.
	D1	NSO0		
	D0	-	-	-
R14 (R0Eh) default “00“h	**Partial non-display area color register 1**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	PSEL	Specifies the color of the partial non-display area	"0" : Displays the color specified in the R15 register. "1" : Displays the most significant bit of the display RAM data. Refer to "5.2 Display Color Selection and Gate Scan Method in Partial Non-Display Areas”.

R15 (“0F“h) default “00“h	**Partial non-display area color register 2**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	PGR	Specifies display data for pixel R.	"0" : Displays "0". "1" : Displays "1".
	D1	PGG	Specifies display data for pixel G.	"0" : Displays "0". "1" : Displays "1".
	D0	PGB	Specifies display data for pixel B.	"0" : Displays "0". "1" : Displays "1".
R16 (R10h) default “00“h	**First display window area starting register 1 , 2**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	P1SL8	Specify the starting line number of the first display window area.	Set within the range of "000"h - "13F"h.
R17 (R11h) default “00“h	D7	P1SL7		
	D6	P1SL6		
	D5	P1SL5		
	D4	P1SL4		
	D3	P1SL3		
	D2	P1SL2		
	D1	P1SL1		
	D0	P1SL0		
R18 (R12h) default “00“h	**Second display window area starting register 1 , 2**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	P2SL8	Specify the starting line number of the second display window area.	Set within the range of "000"h - "13F"h.
R19 (R13h) default “00“h	D7	P2SL7		
	D6	P2SL6		
	D5	P2SL5		
	D4	P2SL4		
	D3	P2SL3		
	D2	P2SL2		
	D1	P2SL1		
	D0	P2SL0		
R20 (R14h) default “00“h	**First display window area display line number 1 , 2**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	P1AW8	Specify the display line number of the first display window area.	Set within the range of "001"h - "140"h.
R21 (R15h) default “00“h	D7	P1AW7		
	D6	P1AW6		
	D5	P1AW5		
	D4	P1AW4		
	D3	P1AW3		
	D2	P1AW2		
	D1	P1AW1		
	D0	P1AW0		

R22 (R16h) default "00"h	**Second display window area display line number 1 , 2**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	P2AW8	Specify the display line number of the second display window area.	Set within the range of 000"h - "13F"h.
R23 (R17h) default "00"h	D7	P2AW7		
	D6	P2AW6		
	D5	P2AW5		
	D4	P2AW4		
	D3	P2AW3		
	D2	P2AW2		
	D1	P2AW1		
	D0	P2AW0		
R24 (R18h) default "00"h	**Power Supply System Control Register 1**			
	D7	VR2ON	Controls the VR2 regulator.	"0" : VR2 regulator off. "1" : VR2 regulator on.
	D6	VR1ON	Controls the VR1 regulator.	"0" : VR1 regulator off. "1" : VR1 regulator on.
	D5	VCLON	Controls the step-up circuit 3 for VCL..	"0" : VCL step-up circuit off. "1" : VCL step-up circuit on.
	D4	VGON	Controls the step-up circuit 2.	"0" : Step-up circuit 2 off. "1" : Step up circuit 2 on.
	D3	-	-	-
	D2	DDVDHON	Controls the step-up circuit 1 for DDVDH.	"0" : DDVDH step-up circuit off. "1" : DDVDH step-up circuit on.
	D1	-	-	-
	D0	DCON	Controls the DC/DC converter.	"0" : DC/DC converter off. "1" : DC/DC converter on.
R25 (R19h) default "00"h	**Power Supply System Control Register 2**			
	D7	VR2SEL2	Specify the output voltage of the VR2 regulator.	-
	D6	VR2SEL1		
	D5	VR2SEL0		
	D4	VR1SEL2	Specify the output voltage of the VR1 regulator.	-
	D3	VR1SEL1		
	D2	VR1SEL0		
	D1	-	-	-
	D0	-	-	-
R26 (R1Ah) default "05"h	**Power Supply System Control Register 3**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	DC3	Specify the step-up circuit 2and 3 frequency	-
	D2	DC2		
	D1	DC1	Specify the step-up circuit 1 frequency	-
	D0	DC0		
R27 (R1Bh) default "0A"h	**Power Supply System Control Register 4**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	VSEL2	Specify the output voltage of the VS and VDH regulator.	-
	D2	VSEL1		
	D1	VSEL0		
	D0	RGON	Controls the VS and VDH regulator.	"0" : VS and VDH regulator off. "1" : VS and VDH regulator on.

R28 (R1Ch) **default "33"h**	**Power Supply System Control Register 5**			
	D7	-	-	-
	D6	SAP2	Source driver circuit operating current control	(SAP2, SAP1, SAP0) = "000": Halt (SAP2, SAP1, SAP0) = "001": 0.5(fixed) (SAP2, SAP1, SAP0) = "010": 0.75(fixed) (SAP2, SAP1, SAP0) = "011": 1.0(fixed) (SAP2, SAP1, SAP0) = "100": 1.25(fixed) (SAP2, SAP1, SAP0) = "101": 1.5(fixed) (SAP2, SAP1, SAP0) = "110": 1.5(fixed) (SAP2, SAP1, SAP0) = "111": Setting disable
	D5	SAP1		
	D4	SAP0		
	D3	-	-	-
	D2	AP2	Step-up circuit operating current control	(AP2, AP1, AP0) = "000": Halt (AP2, AP1, AP0) = "001": Setting disable (AP2, AP1, AP0) = "010": 0.5(fixed) (AP2, AP1, AP0) = "011": 0.75(fixed) (AP2, AP1, AP0) = "100": 1.0(fixed) (AP2, AP1, AP0) = "101": 1.25(fixed) (AP2, AP1, AP0) = "110": 1.5(fixed) (AP2, AP1, AP0) = "111": Setting disable
	D1	AP1		
	D0	AP0		
R29 (R1Dh) **default "03"h**	**Power Supply System Control Register 6**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	R/L	Specifies the gate scan direction.	-
	D2	SCN2	Specify gate scan mode.	(SCN2, SCN1, SCN0) = "XX0" : MODE5 (SCN2, SCN1, SCN0) = "011" : MODE2
	D1	SCN1		
	D0	SCN0		
R30 (R1Eh) **default "00"h**	**Power Supply System Control Register 8**			
	D7	VCOMEN	Specify the VCOM1 operation.	-
	D6			
	D5	VCOMFX		
	D4	VCOMHI		
	D3	XVCOMG	VCOML output control	"0": VCOML is setting by VDV and VCM bits "1": VCOML = VSSA
	D2	-	-	-
	D1	-	-	-
	D0	DDVDHXON	Specifies whether to use or not to use the extra step-up circuit 1 for DDVDH.	"0" : Doesn't use the extra step-up circuit 1. "1" : Uses the extra step-up circuit 1.
R31 (R1Fh) **default "00"h**	**Power Supply System Control Register 9**			
	D7	-	Specify the VCOM amplitude.	-
	D6	-		
	D5	-		
	D4	VDV4		
	D3	VDV3		
	D2	VDV2		
	D1	VDV1		
	D0	VDV0		
R32 (R20h) **default "00"h**	**Power Supply System Control Register 10**			
	D7	-	Specify the VCOMH voltage level	-
	D6	-		
	D5	-		
	D4	VCM4		
	D3	VCM3		
	D2	VCM2		
	D1	VCM1		
	D0	VCM0		

R36 (R24h) default "73"h	**Power Supply System Control Register 11**			
	D7	-	-	-
	D6	IBV2	Specify the constant current source of V18 regulator.	(IBV2, IBV1, IBV0) = "000": 0.2 (IBV2, IBV1, IBV0) = "001": 0.4 (IBV2, IBV1, IBV0) = "010": 0.6 (IBV2, IBV1, IBV0) = "011": 0.8 (IBV2, IBV1, IBV0) = "100": Setting disable (IBV2, IBV1, IBV0) = "101": Setting disable (IBV2, IBV1, IBV0) = "110": Setting disable (IBV2, IBV1, IBV0) = "111": 1
	D5	IBV1		
	D4	IBV0		
	D3	-	-	-
	D2	BIAS2	Specify the constant current source of VCOM regulator	(BIAS2, BIAS1, BIAS0) = "000": Halt (BIAS2, BIAS1, BIAS0) = "001": Setting disable (BIAS2, BIAS1, BIAS0) = "010": 0.5 (BIAS2, BIAS1, BIAS0) = "011": 0.75 (BIAS2, BIAS1, BIAS0) = "100": 1 (BIAS2, BIAS1, BIAS0) = "101": 1.25 (BIAS2, BIAS1, BIAS0) = "110": 1.5 (BIAS2, BIAS1, BIAS0) = "111": Setting disable
	D1	BIAS1		
	D0	BIAS0		
R37 (R25h) default "00"h	**Power Supply System Control Register 12**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	BT3	Specify the step-up factor in step up circuit 2.	-
	D2	BT2		
	D1	BT1		
	D0	BT0		
R40 (R28h) default "25"h	**Power Supply System Control Register 14**			
	D7	DCCLK7	Specify the frequency for the DC/DC converter (DCDCf)	DCDCf = SYSCLK / DCCLK
	D6	DCCLK6		
	D5	DCCLK5		
	D4	DCCLK4		
	D3	DCCLK3		
	D2	DCCLK2		
	D1	DCCLK1		
	D0	DCCLK0		
R43 (R2Bh) default "00"h	**OSC resistance control**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	RADJ2	Internal oscillator frequency correction function	(RADJ2, RADJ1, RADJ0) = "000": No correction (RADJ2, RADJ1, RADJ0) = "001": -10% (RADJ2, RADJ1, RADJ0) = "010": -20% (RADJ2, RADJ1, RADJ0) = "011": -30% (RADJ2, RADJ1, RADJ0) = "100": +10% (RADJ2, RADJ1, RADJ0) = "101": +20% (RADJ2, RADJ1, RADJ0) = "110": +30% (RADJ2, RADJ1, RADJ0) = "111": +40%
	D2	RADJ1		
	D1	RADJ0		
	D0	ROSC	Specify the oscillation resister mode	"0": External resister mode "1": Internal resister mode
R45 (R2Dh) default "01"h	**Calibration register**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	OC	Execute calibration.	"0" : Starts calibration "1" : Stops calibration. Refer to "3.3 Internal Clock Mode"

R49 (R31h)	**ID code register 1**			
	D7	MCOD3	Manufacturer code.	-
	D6	MCOD2		
	D5	MCOD1		
	D4	MCOD0		
default "01"h	D3	VCOD3	The version of this LSI.	Depends on the version of the product.
	D2	VCOD2		
	D1	VCOD1		
	D0	VCOD0		
R50 (R32h)	-	-	-	**ID code register 2**
	D7	DCOD7	Device code of this LSI.	-
	D6	DCOD6		
	D5	DCOD5		
	D4	DCOD4		
default "0C"h	D3	DCOD3		
	D2	DCOD2		
	D1	DCOD1		
	D0	DCOD0		
R51 (R33h)	D7	**N line inversion register**		
	D6	NLINE6	Specify the number of lines for N line inversion.	Set within the range of "01"h - "78"h. Refer to "7 Gate Line Driving Function".
	D5	NLINE5		
	D4	NLINE4		
default "01"h	D3	NLINE3		
	D2	NLINE2		
	D1	NLINE1		
	D0	NLINE0		
R52 (R34h)	**Partial gate register 1**			
	D7	GSMLN7	Specify the gate scanning cycle of the non-display area	"00"h : Doesn't scan the partial non-display area. "01"h : Scans the partial non-display area every frame. "02"h : Scans the partial non-display area every two frames.
	D6	GSMLN6		
	D5	GSMLN5		
	D4	GSMLN4		
default "01"h	D3	GSMLN3		
	D2	GSMLN2		
	D1	GSMLN1		
	D0	GSMLN0		
R53 (R35h)	**Partial gate register 2**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
default "00"h	D1	-	-	-
	D0	PNFRM	Configures the driving method of the partial non-display area.	"0" : The partial non-display area is driven as that in the partial display area. "1" : The partial non-display area is driven by the frame inversion.
R55 (R37h)	**Gate scan selection register**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
default "00"h	D3	-	-	
	D2	GSCAN2	Select the method of gate scanning.	-
	D1	GSCAN1		
	D0	GSCAN0		
R59 (R3Bh)	**Gate output control register**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
default "00"h	D2	-	-	-
	D1	-	-	-
	D0	DISPTMG	Controls the gate output	"0" : Fix all gate outputs to VGL level. "1" : Gate scanning normal operation.

R60 (R3Ch) default "00"h	**RGB start line register 1 , 2**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	RGBST8	Specify the display start line in the RGB interface circuit.	-
R61 (R3Dh) default "00"h	D7	RGBST7		
	D6	RGBST6		
	D5	RGBST5		
	D4	RGBST4		
	D3	RGBST3		
	D2	RGBST2		
	D1	RGBST1		
	D0	RGBST0		
R62 (R3Eh) default "00"h	**RGB end line register 1 , 2**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	RGBED8	Specify the display end line in the RGB interface circuit.	-
R63 (R3Fh) default "00"h	D7	RGBED7		
	D6	RGBED6		
	D5	RGBED5		
	D4	RGBED4		
	D3	RGBED3		
	D2	RGBED2		
	D1	RGBED1		
	D0	RGBED0		
R64 (R40h) default "02"h	**Horizontal back porch setting register**			
	D7	-	-	-
	D6	-	-	-
	D5	HBP5	Specify the horizontal back porch period in the RGB interface circuit.	-
	D4	HBP4		
	D3	HBP3		
	D2	HBP2		
	D1	HBP1		
	D0	HBP0		
R65 (R41h) default "02"h	**Vertical back porch setting register**			
	D7	-	-	-
	D6	-	-	-
	D5	VBP5	Specify the vertical back porch period in the RGB interface circuit	
	D4	VBP4		
	D3	VBP3		
	D2	VBP2		
	D1	VBP1		
	D0	VBP0		
R66 (R42h) default "00"h	**X address register**			
	D7	XA7	Specify the X-starting address of the display RAM.	Set within the range of "00"h - "EF"h.
	D6	XA6		
	D5	XA5		
	D4	XA4		
	D3	XA3		
	D2	XA2		
	D1	XA1		
	D0	XA0		

	Y address register			
R67 (R43h)	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
default "00"h	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	YA8	Specify the Y-starting address of the display RAM	Set within the range of "000"h - "13F"h.
R68 (R44h)	D7	YA7		
	D6	YA6		
	D5	YA5		
	D4	YA4		
	D3	YA3		
default "00"h	D2	YA2		
	D1	YA1		
	D0	YA0		
	MIN X address register			
R69 (R45h)	D7	XMIN7	Specify X start address for the window area access mode.	Set within the range of "00"h - "EF"h.
	D6	XMIN6		
	D5	XMIN5		
	D4	XMIN4		
default "00"h	D3	XMIN3		
	D2	XMIN2		
	D1	XMIN1		
	D0	XMIN0		
	MAX X address register			
R70 (R46h)	D7	XMX7	Specify X end address for the window area access mode.	Set within the range of "00"h - "EF"h.
	D6	XMX6		
	D5	XMX5		
	D4	XMX4		
default "00"h	D3	XMX3		
	D2	XMX2		
	D1	XMX1		
	D0	XMX0		
	MIN Y address register			
R71 (R47h)	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
default "00"h	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	YMIN8	Specify the Y start address for the window area access mode	Set within the range of "000"h -"13F"h
R72 (R48h)	D7	YMIN7		
	D6	YMIN6		
	D5	YMIN5		
	D4	YMIN4		
default "00"h	D3	YMIN3		
	D2	YMIN2		
	D1	YMIN1		
	D0	YMIN0		

R73 (R49h) default "00"h	**MAX Y address register**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	YMX8	Specify the Y end address for the window area access mode	Set within the range of "000"h -"13F"h
R74 (R4Ah) default "00"h	D7	YMX7		
	D6	YMX6		
	D5	YMX5		
	D4	YMX4		
	D3	YMX3		
	D2	YMX2		
	D1	YMX1		
	D0	YMX0		
R75 (R4Bh) default "00"h	**Scroll area start register 1, 2**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	SSL8	Specify the scroll start line address	Set within the range of "000"h -"13F"h
R76 (R4Ch) default "00"h	D7	SSL7		
	D6	SSL6		
	D5	SSL5		
	D4	SSL4		
	D3	SSL3		
	D2	SSL2		
	D1	SSL1		
	D0	SSL0		
R77 (R4Dh) default "00"h	**Scroll area line number register 1, 2**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	SAW8	Specify the scroll area line number	Set within the range of "000"h -"13F"h
R78 (R4Eh) default "00"h	D7	SAW7		
	D6	SAW6		
	D5	SAW5		
	D4	SAW4		
	D3	SAW3		
	D2	SAW2		
	D1	SAW1		
	D0	SAW0		

	Scroll area step number register 1, 2			
R79 (R4Fh)	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
default "00"h	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	SST8	Specify the number of lines to be scrolled (amount of scrolling)	Set within the range of "000"h-"13F"h.
R80 (R50h)	D7	SST7		
	D6	SST6		
	D5	SST5		
	D4	SST4		
default "00"h	D3	SST3		
	D2	SST2		
	D1	SST1		
	D0	SST0		
R118 (R76h)				
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
default "00"h	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	DMYSEL	Specify the number of dummy lines	"0" : 1 line refer to "10.2 Blanking Period and Dummy Line "1" : 8 line Location"
Gate on interval control register				
R134 (R86h)	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
default "00"h	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	GOF8	Specify the gate line output off timing.	-
R135 (R87h)	D7	GOF7		GOF = GON + Gate output period 1) Set GOF by the SYSCLK number in the internally synchronized display mode. 2) Set GOF by the Dotclk number / 8 in the externally synchronized display mode.
	D6	GOF6		
	D5	GOF5		
	D4	GOF4		
default "20"h	D3	GOF3		
	D2	GOF2		
	D1	GOF1		
	D0	GOF0		
Source on interval control register				
R136 (R88h)	D7	SON7	Specify the source line output on timing.	Set the time from the horizontal period by the SYSCLK number.
	D6	SON6		
	D5	SON5		
	D4	SON4		
default "02"h	D3	SON3		
	D2	SON2		
	D1	SON1		
	D0	SON0		
Gate on interval control register				
R137 (R89h)	D7	GON7	Specify the gate line output off timing.	GON is the time from the starting of the horizontal scan. 1) Set GON by the SYSCLK number in the internally synchronized display mode. 2) Set GON by the Dotclk number / 8 in the externally synchronized display mode.
	D6	GON6		
	D5	GON5		
	D4	GON4		
default "03"h	D3	GON3		
	D2	GON2		
	D1	GON1		
	D0	GON0		

Line clock register 1				
R139 (R8Bh) **default “25“h**	D7	HCK7	Specify the period for the number of 1 horizontal period.	R141: CLKM=0 => a calibrated clock number is written. R141: CLKM=1 => Set a raster-row clock number; the integer of HCK close to a target frame frequency calculated with SYSCLK number. *Note: This HCK setting is invalid when CLKM=0.
	D6	HCK6		
	D5	HCK5		
	D4	HCK4		
	D3	HCK3		
	D2	HCK2		
	D1	HCK1		
	D0	HCK0		
Line clock register 2				
R140 (R8Ch) **default “25“h**	D7	HCK7	A register to read the R139 data.	The data of R139 is copied to this register automatically. The MPU can read the same data as R139.
	D6	HCK6		
	D5	HCK5		
	D4	HCK4		
	D3	HCK3		
	D2	HCK2		
	D1	HCK1		
	D0	HCK0		
Line frequency control register				
R141 (R8Dh) **default “00“h**	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	CLKM	Specifies the line frequency control mode.	"0" : Calibration mode. "1" : Register set-up mode.
Gamma control register 1				
R143 (R8Fh) **default “00“h**	D7		Gamma adjustment register	-
	D6	MP12		
	D5	MP11		
	D4	MP10		
	D3	-		
	D2	MP02		
	D1	MP01		
	D0	MP00		
Gamma control register 2				
R144 (R90h) **default “00“h**	D7	-	Gamma adjustment register	-
	D6	MP32		
	D5	MP31		
	D4	MP30		
	D3	-		
	D2	MP22		
	D1	MP21		
	D0	MP20		
Gamma control register 3				
R145 (R91h) **default “00“h**	D7	-	Gamma adjustment register	-
	D6	MP52		
	D5	MP51		
	D4	MP50		
	D3	-		
	D2	MP42		
	D1	MP41		
	D0	MP40		
Gamma control register 4				
R146 (R92h) **default “00“h**	D7	-	Gamma adjustment register	-
	D6	CP12		
	D5	CP11		
	D4	CP10		
	D3	-		
	D2	CP02		
	D1	CP01		
	D0	CP00		

Gamma control register 5				
R147 (R93h)	D7	-	Gamma adjustment register	-
	D6	MN12		
	D5	MN11		
	D4	MN10		
	D3	-		
default “00“h	D2	MN02		
	D1	MN01		
	D0	MN00		
Gamma control register 6				
R148 (R94h)	D7	-	Gamma adjustment register	-
	D6	MN32		
	D5	MN31		
	D4	MN30		
	D3	-		
default “00“h	D2	MN22		
	D1	MN21		
	D0	MN20		
Gamma control register 7				
R149 (R95h)	D7	-	Gamma adjustment register	-
	D6	MN52		
	D5	MN51		
	D4	MN50		
	D3	-		
default “00“h	D2	MN42		
	D1	MN41		
	D0	MN40		
Gamma control register 8				
R150 (R96h)	D7	-	Gamma adjustment register	-
	D6	CN12		
	D5	CN11		
	D4	CN10		
	D3	-		
default “00“h	D2	CN02		
	D1	CN01		
	D0	CN00		
Gamma control register 9				
R151 (R97h)	D7	-	Gamma adjustment register	-
	D6	-		
	D5	-		
	D4	-		
	D3	OP03		
default “00“h	D2	OP02		
	D1	OP01		
	D0	OP00		
Gamma control register 10				
R152 (R98h)	D7	-	Gamma adjustment register	-
	D6	-		
	D5	-		
	D4	OP14		
	D3	OP13		
default “00“h	D2	OP12		
	D1	OP11		
	D0	OP10		
Gamma control register 11				
R153 (R99h)	D7	-	Gamma adjustment register	-
	D6	-		
	D5	-		
	D4	-		
	D3	ON03		
default “00“h	D2	ON02		
	D1	ON01		
	D0	ON00		

Gamma control register 12				
R154 (R9Ah) **default "00"h**	D7	-	Gamma adjustment register	-
	D6	-		
	D5	-		
	D4	ON14		
	D3	ON13		
	D2	ON12		
	D1	ON11		
	D0	ON10		
Extend mode register				
R157 (R9Dh) **default "00"h**	D7	-	-	-
	D6	-	-	-
	D5	MON_EN	Specify the V0 and V63 monitor function	"0": V0 and V63 output monitor is disable. "1": V0 and V63 output monitor is enable.
	D4	MON_SEL	V0 and V63 monitor selection	"0": V0 outputs at DS1 pin. "1": V63 outputs at DS1 pin
	D3	-	-	-
	D2	BPEN	Specify the Enable operation	"0": Enable control is available. "1": VBP/HBP control is enable
	D1	EPL	Specify the Enable polarity	"0": High active "1": Low active
	D0	MSBF	NWRGB (R2:D0)="1"	"0" : 18-bit x 1transfer (BWS2="L"). RGB interface type RGB1 "0" : 16-bit x 1transfer (BWS2="H"). RGB interface type RGB2 "1" : 6-bit x 3 transfer (BWS2=x). RGB interface type RGB3
			NWRGB (R2:D0)="0"	"0" : MPU5 mode A (use lower 6bits). MPU interface type "1" : MPU5 mode B (use upper 6bits). MPU interface type This bit is invalid in other modes.
Off mode register				
R192 ("C0"h) **default "00"h**	D7	OFFMOD	Specify the Off mode	"0": Normal mode "1": Off mode In off mode, only OFFMOD bit can be updated. Other register and the display RAM can not be updated. The display RAM data may not be retained in off mode, and need to rewrite after off mode canceling.
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	-	-	-
RGB mode register				
R193 ("C1"h) **default "01"h**	D7			
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	BGR	Specify the order of <R><G><B> dot color in one pixel stored in display RAM.	When BGR = 1, the order sent from the MPU with expanding to 18 bits are reversed bit order from <R><G><B> order to <B><G><R> order.

17. Electrical Characteristic

17.1 Absolute Maximum Ratings

The absolute maximum ratings are list on Table 17.1. When used out of the absolute maximum ratings, the LSI may be permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the LSI will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power Supply Voltage (1)	VCC,IOVCC	V	-0.3 to +4.6	1,2
Power Supply Voltage (2)	VCI ~ VSSA	V	-0.3 to +4.6	1,2
Power Supply Voltage (3)	VLCD ~ VSSA	V	-0.3 to +6.0	3
Power Supply Voltage (4)	VSSA ~ VCL	V	-0.3 to +4.6	4
Power Supply Voltage (5)	VLCD ~ VCL	V	-0.3 to +9	5
Power Supply Voltage (6)	VGH ~ VSSA	V	-0.3 to +18.5	6
Power Supply Voltage (7)	VSSA ~ VGL	V	0 to -16.5	7
Input Voltage	Vi	V	-0.3 to VCC+0.3	-
Operating Temperature	Topr	°C	-40 to +85	8,9
Storage Temperature	Tstg	°C	-55 to +110	8,9

Table 17. 1 Absolute maximum rating

Note:
1.VCC, VSSD must be maintained.
2.To make sure IOVCC ≥ VSSD.
3.To make sure VCI ≥ VSSA.
4.To make sure VLCD ≥ VSSA.
5.To make sure VLCD ≥ VCL.
6.To make sure VGH ≥ VSSA.
7.To make sure VSSA ≥ VGL
VGH +|VGL| < 32V
8.For die and wafer products, specified up to +85℃.
9.This temperature specifications apply to the TCP package.

17.2 AC Characteristic

Clock Characteristics (VCC = 2.2 ~ 3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
External clock frequency	f_{cp}	MHz	-	1.2	-	VCC= 2.4 ~ 3.3V
External clock duty ratio	Duty	%	45	50	55	VCC= 2.4 ~ 3.3V
External clock rise time	Trcp	µs	-	-	0.2	VCC= 2.4 ~ 3.3V
External clock fall time	Tfcp	µs	-	-	0.2	VCC= 2.4 ~ 3.3V
R-C oscillation clock	f_{OSC}	MHz	-	1.2	-	Rf = 100K Ω , VCC=2.8V

80-system Bus Interface Timing Characteristics

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	200	-	-	Figure 17.1
	Read	t_{CYCR}	ns	300	-	-	Figure 17.1
Write low-level pulse width		PW_{LW}	ns	40	-	-	Figure 17.1
Read low-level pulse width		PW_{LR}	ns	150	-	-	Figure 17.1
Write high-level pulse width		PW_{HW}	ns	70	-	-	Figure 17.1
Read high-level pulse width		PW_{HR}	ns	150	-	-	Figure 17.1
Write / Read rise / fall time		t_{WRr} , t_{WRf}	ns	-	-	25	Figure 17.1
RS Setup time	(RS to NCS, NWR)	t_{AS}	ns	5	-	-	Figure 17.1
RS hold time	(NCS, NWR to RS)	t_{AH}	ns	5	-	-	Figure 17.1
Write data set up time		t_{DSW}	ns	20	-	-	Figure 17.1
Write data hold time		t_H	ns	15	-	-	Figure 17.1
Read data delay time		t_{DDR}	ns	-	-	100	Figure 17.1
Read data hold time		t_{DHR}	ns	5	-	-	Figure 17.1

Table 17. 3. 1 Normal Write Mode (IOVCC = 1.65 ~ 2.4V) / (VCC = 2.4V~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	125	-	-	Figure 17.1
	Read	t_{CYCR}	ns	300	-	-	Figure 17.1
Write low-level pulse width		PW_{LW}	ns	40	-	-	Figure 17.1
Read low-level pulse width		PW_{LR}	ns	150	-	-	Figure 17.1
Write high-level pulse width		PW_{HW}	ns	70	-	-	Figure 17.1
Read high-level pulse width		PW_{HR}	ns	150	-	-	Figure 17.1
Write / Read rise / fall time		t_{WRr} , t_{WRf}	ns	-	-	25	Figure 17.1
RS Setup time	(RS to NCS, NWR)	t_{AS}	ns	5	-	-	Figure 17.1
RS hold time	(NCS, NWR to RS)	t_{AH}	ns	5	-	-	Figure 17.1
Write data set up time		t_{DSW}	ns	20	-	-	Figure 17.1
Write data hold time		t_H	ns	15	-	-	Figure 17.1
Read data delay time		t_{DDR}	ns	-	-	100	Figure 17.1
Read data hold time		t_{DHR}	ns	5	-	-	Figure 17.1

Table 17. 3. 2 Normal Write Mode (IOVCC = 2.4 ~ 3.3V) / (VCC = 2.4V~3.3V)

68-system Bus Interface Timing Characteristics

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCEW}	ns	200	-	-	Figure 17.2
	Read	t_{CYCER}	ns	300	-	-	Figure 17.2
Write low-level pulse width		PWE_{LW}	ns	70	-	-	Figure 17.2
Read low-level pulse width		PWE_{LR}	ns	150	-	-	Figure 17.2
Write high-level pulse width		PWE_{HW}	ns	40	-	-	Figure 17.2
Read high-level pulse width		PWE_{HR}	ns	150	-	-	Figure 17.2
Write / Read rise / fall time		t_{WRr} , t_{WRf}	ns	-	-	25	Figure 17.2
RS setup time	(RS to NCS, E)	t_{ASE}	ns	5	-	-	Figure 17.2
RS hold time	(NCS, E to RS)	t_{AHE}	ns	5	-	-	Figure 17.2
Write data set up time		t_{DSWE}	ns	20	-	-	Figure 17.2
Write data hold time		t_{HE}	ns	15	-	-	Figure 17.2
Read data delay time		t_{DDR}	ns	-	-	100	Figure 17.2
Read data hold time		t_{DHR}	ns	5	-	-	Figure 17.2

Table 17. 4. 1 Normal Write Mode (IOVCC = 1.65 ~ 2.4V) / (VCC = 2.4V~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCEW}	ns	125	-	-	Figure 17.2
	Read	t_{CYCER}	ns	300	-	-	Figure 17.2
Write low-level pulse width		PWE_{LW}	ns	70	-	-	Figure 17.2
Read low-level pulse width		PWE_{LR}	ns	200	-	-	Figure 17.2
Write high-level pulse width		PWE_{HW}	ns	40	-	-	Figure 17.2
Read high-level pulse width		PWE_{HR}	ns	200	-	-	Figure 17.2
Write / Read rise / fall time		t_{WRr} , t_{WRf}	ns	-	-	25	Figure 17.2
Setup time	Write (RS to NCS, E_NWR)	t_{ASE}	ns	10	-	-	Figure 17.2
	Read (RS to NCS , RW_NRD)			10	-	-	Figure 17.2
Address hold time		t_{AHE}	ns	5	-	-	Figure 17.2
Write data set up time		t_{DSWE}	ns	60	-	-	Figure 17.2
Write data hold time		t_{HE}	ns	15	-	-	Figure 17.2
Read data delay time		t_{DDR}	ns	-	-	100	Figure 17.2
Read data hold time		t_{DHR}	ns	5	-	-	Figure 17.2

Table 17. 4. 2 Normal Write Mode (IOVCC = 2.4 ~ 3.3V) / (VCC = 2.4V~3.3V)

Serial Data Transfer Interface Timing Characteristics

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write (received)	t_{SCYC}	ns	100	-	-	Figure 17.3
	Read (transmitted)	t_{SCYC}	ns	200	-	-	Figure 17.3
Serial clock high – level pulse width	Write (received)	t_{SCH}	ns	40	-	-	Figure 17.3
	Read (transmitted)	t_{SCH}	ns	150	-	-	Figure 17.3
Serial clock low – level pulse width	Write (received)	t_{SCL}	ns	40	-	-	Figure 17.3
	Read (transmitted)	t_{SCL}	ns	150	-	-	Figure 17.3
Serial clock rise / fall time		t_{scr} , t_{scf}	ns	-	-	20	Figure 17.3
Chip select (NCS) set up time		t_{CSU}	ns	20	-	-	Figure 17.3
Chip select (NCS) hold time		t_{CH}	ns	60	-	-	Figure 17.3
RS set up time		t_{RSU}	ns	10			Figure 17.3
RS hold time		t_{RSH}	ns	10			Figure 17.3
Read/write select (RNW) set up time		t_{WRU}	ns	10			Figure 17.3
Read/write select (RNW) hold time		t_{WRH}	ns	10			Figure 17.3
Read clock set up time		t_{SCSR}	ns	10			Figure 17.3
Read clock hold time		t_{SCHR}	ns	10			Figure 17.3
Serial input data set up time		t_{SISU}	ns	30	-	-	Figure 17.3
Serial input data hold time		t_{SIH}	ns	30	-	-	Figure 17.3
Serial output data delay time		t_{SOD}	ns	-	-	100	Figure 17.3
Serial output data hold time		t_{SOH}	ns	5	-	-	Figure 17.3

Table 17. 5. 1 (IOVCC=1.65~3.3V) / (VCC = 2.4V~3.3V)

RGB Interface Timing Characteristics

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC / HSYNC set up time	t_{SYNCS}	ns	10	-	-	Figure 17.4
ENABLE set up time	t_{ENS}	ns	10	-	-	Figure 17.4
ENABLE hold time	t_{ENH}	ns	10	-	-	Figure 17.4
DOTCLK “low” level pulse width	PW_{DL}	ns	40	-	-	Figure17.4
DOTCLK “high” level pulse width	PW_{DH}	ns	40	-	-	Figure17.4
DOTCLK cycle time	t_{CYCD}	ns	200	-	-	Figure17.4
DATA set up time	t_{PDS}	ns	20	-	-	Figure17.4
DATA hold time	t_{PDH}	ns	20	-	-	Figure17.4
DOTCLK , VSYNC , HSYNC rising and falling time	t_{rgbr} , t_{rgbf}	ns	-	-	25	Figure17.4

Table 17. 6. 1 RGB interface mode, Normal Write Mode (IOVCC=1.65~2.4V) / (VCC = 2.4V~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC / HSYNC set up time	t_{SYNCS}	ns	10	-	-	Figure 17.4
ENABLE set up time	t_{ENS}	ns	10	-	-	Figure 17.4
ENABLE hold time	t_{ENH}	ns	10	-	-	Figure 17.4
DOTCLK “low” level pulse width	PW_{DL}	ns	40	-	-	Figure 17.4
DOTCLK “high” level pulse width	PW_{DH}	ns	40	-	-	Figure 17.4
DOTCLK cycle time	t_{CYCD}	ns	150	-	-	Figure 17.4
DATA set up time	t_{PDS}	ns	20	-	-	Figure 17.4
DATA hold time	t_{PDH}	ns	20	-	-	Figure 17.4
DOTCLK , VSYNC , HSYNC rising and falling time	t_{rgbr} , t_{rgbf}	ns	-	-	25	Figure 17.4

Table 17. 6. 2 RGB interface mode, Normal Write Mode (IOVCC=2.4~3.3V) / (VCC = 2.4V~3.3V)

17.3 LCD driver output Characteristics

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Driver output delay timing	t_{DD}	us	-	25	-	**Figure 17.5** VCI=IOVCC=VCC=2.8V , Ta=25°C , fOSC = 930KHz, (320 Line) VBP=02h , VFP =02h, Black Image, Frame rate = 60Hz, SAP=111,AP=011,HCK=30h,DCCLK=18h, DC=0101,NLINE=000001, VR1SEL=000, VR2SEL=000, VSEL=100, BT=0101, VRH=0011, VCM=10000, VDV=10001, XVCOMG=0, DDVDHXON=1, COLOR=0.

Table 17.7 Driver output delay timing

17.4 Reset Timing Characteristics

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Reset low level width	t_{RES}	ms	1	-	-	Figure17.5
Reset rise time	t_{rRES}	ns	-	-	10	Figure17.5

Table 17.8 (IOVCC=1.65~3.3V) / (VCC = 2.4V~3.3V)

17.5 DC Characteristic

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V_{IH}	V	IOVCC= 1.65 ~ 3.3V	0.8xIOVCC	-	IOVCC	-
Input low voltage	V_{IL}	V	IOVCC= 1.65 ~ 3.3V	-0.3V	-	0.2xIOVCC	-
Output high voltage(1) (DB17-0, SDO Pins)	V_{OH1}	V	I_{OH} = -0.1 mA	0.8xIOVCC	-	-	-
Output low voltage (DB17-0, SDO Pins)	V_{OL1}	V	IOVCC= 1.65 ~ 3.3V I_{OL} = 0.1mA	-	-	0.2xIOVCC	-
I/O leakage current	I_{Li}	µA	Vin = 0 ~ VCC	-1	-	1	-
Current consumption during normal operation (VCC – VSSD)+ (IOVCC-VSSD)	$I_{OP(VCC)}$	µA	VCI=IOVCC=VCC=2.8V, Ta=25°C , fOSC = 930KHz, (320 Line) VBP=02h , VFP =02h, Black Image, Frame rate = 60Hz, SAP=111,AP=011,HCK=30h, DCCLK=18h, DC=0101, NLINE=000001, VR1SEL=000, VR2SEL=000, VSEL=100, BT=0101, VRH=0011,VCM=10000, VDV=10001, XVCOMG=0, DDVDHXON=1, COLOR=0. No panel load	-	450	700	-
Current consumption during normal operation (VCI – VSSD)	$I_{OP(Vci)}$	mA			2.2	2.7	
Current consumption during standby mode (VCC – VSSD) + (IOVCC-VSSD)	$I_{ST(VCC)}$	µA	VCC=VCI=2.8V , Ta=25°C	-	5	10	-
Current consumption during standby mode (VCI – VSSD)	$I_{ST(VCi)}$	µA			0.5	1	
Current consumption during OFF mode (VCC – VSSD) + (IOVCC-VSSD)	$I_{ST(VCC)}$	µA	VCC=VCI=2.8V , Ta=25°C		1	5	
Current consumption during OFF mode (VCI – VSSD)	$I_{ST(VCi)}$	µA			0.5	1	
Output voltage deviation	-	mV	-	-	5	-	-
Dispersion of the Average Output Voltage	V	mV	-	-	-	35	-

Table 17. 9 DC Characteristic (VCC = 2.4 ~ 3.3V, IOVCC = 1.8 ~3.3V, Ta = -40 ~ 85 °C)

17.6 Timing Characteristic

80-system Bus Operation

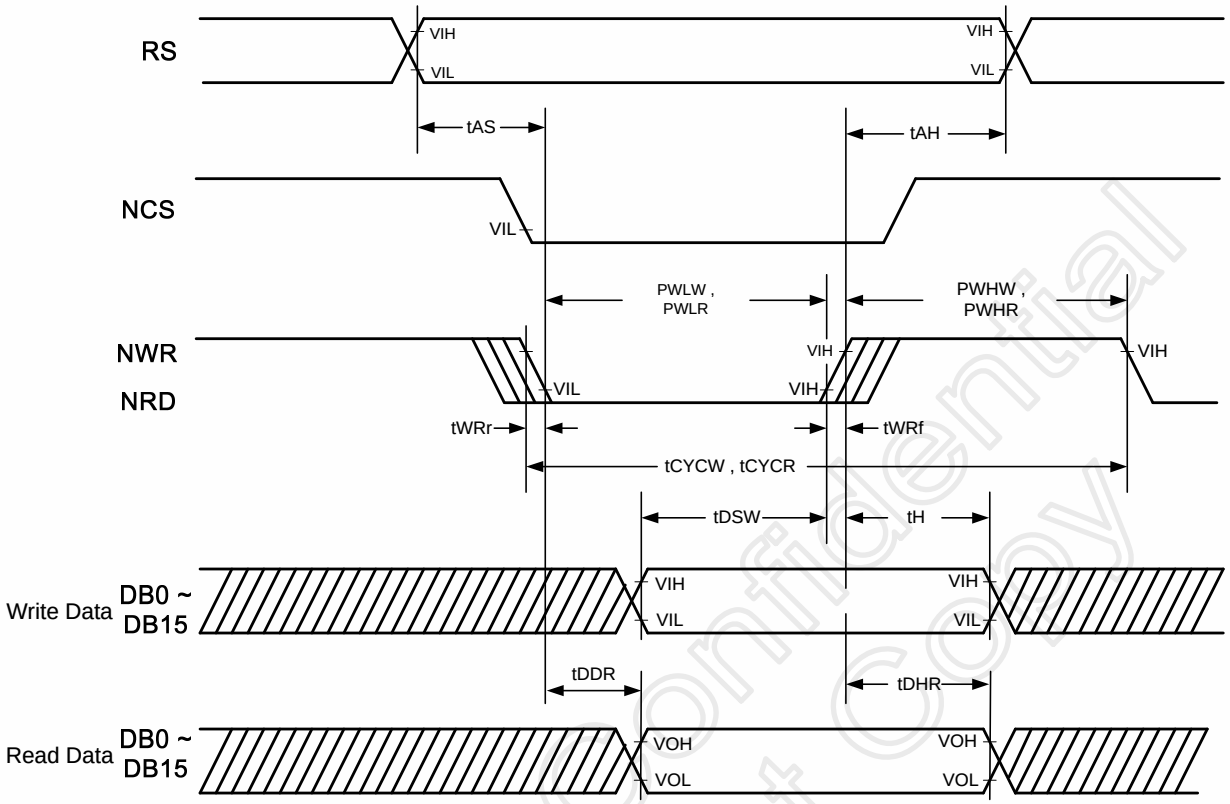


Figure 17. 1 80-system Bus Timing

68-system Bus Operation

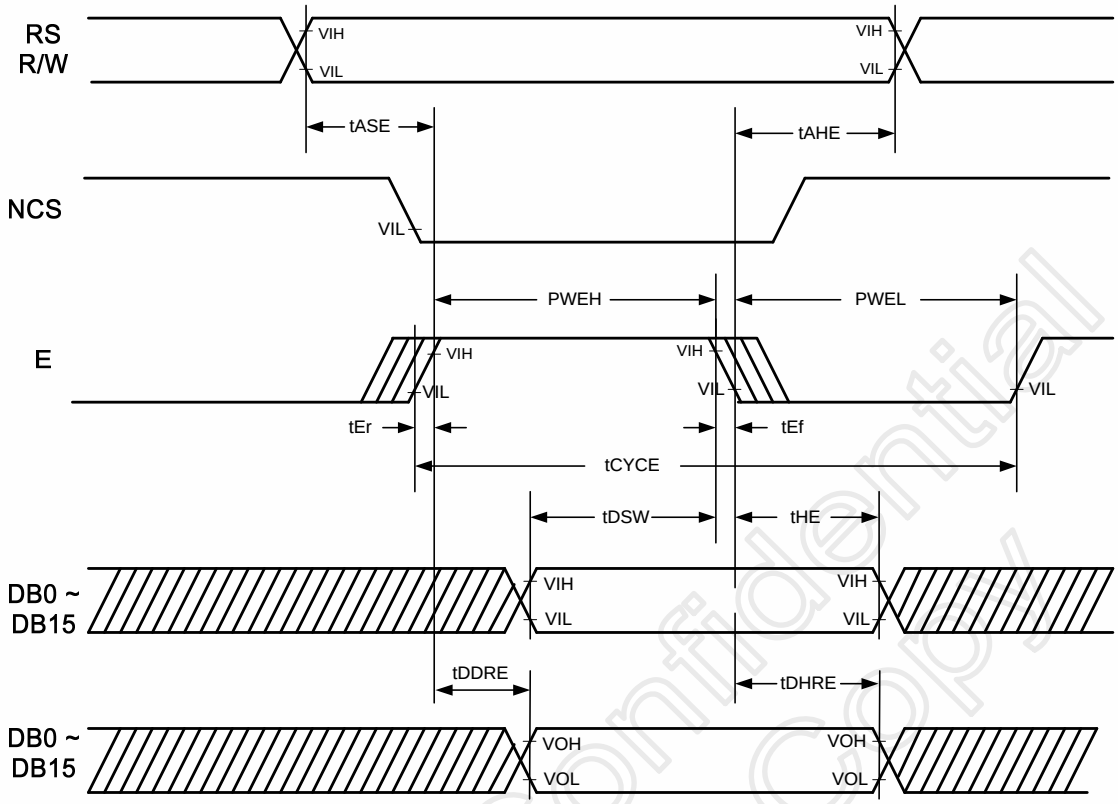


Figure 17. 2 68-System Bus Timing

Clock Synchronized Serial Data Transfer Interface Operation

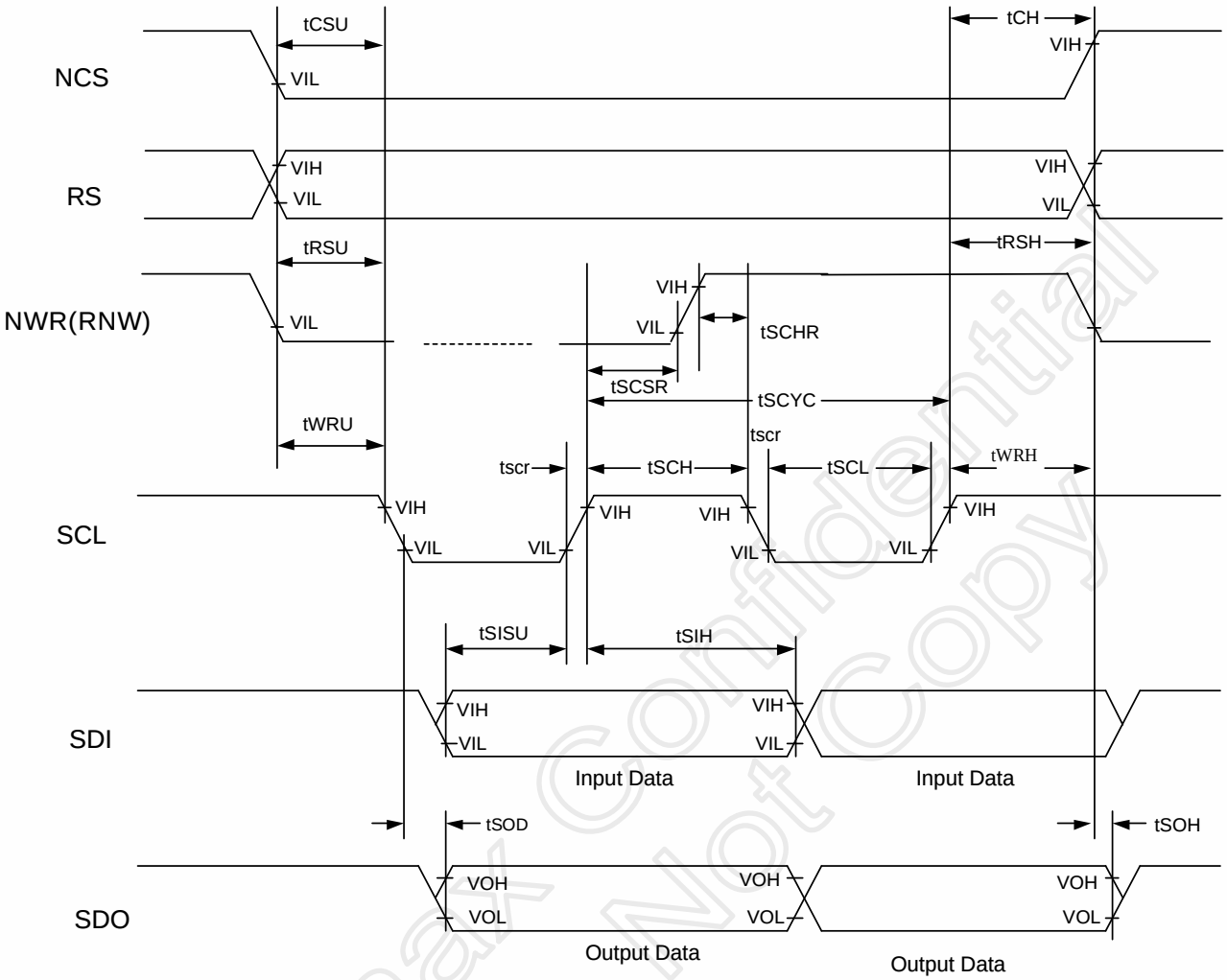


Figure 17. 3 Clock Synchronized Serial Data Transfer Interface Timing

RGB Interface Operation

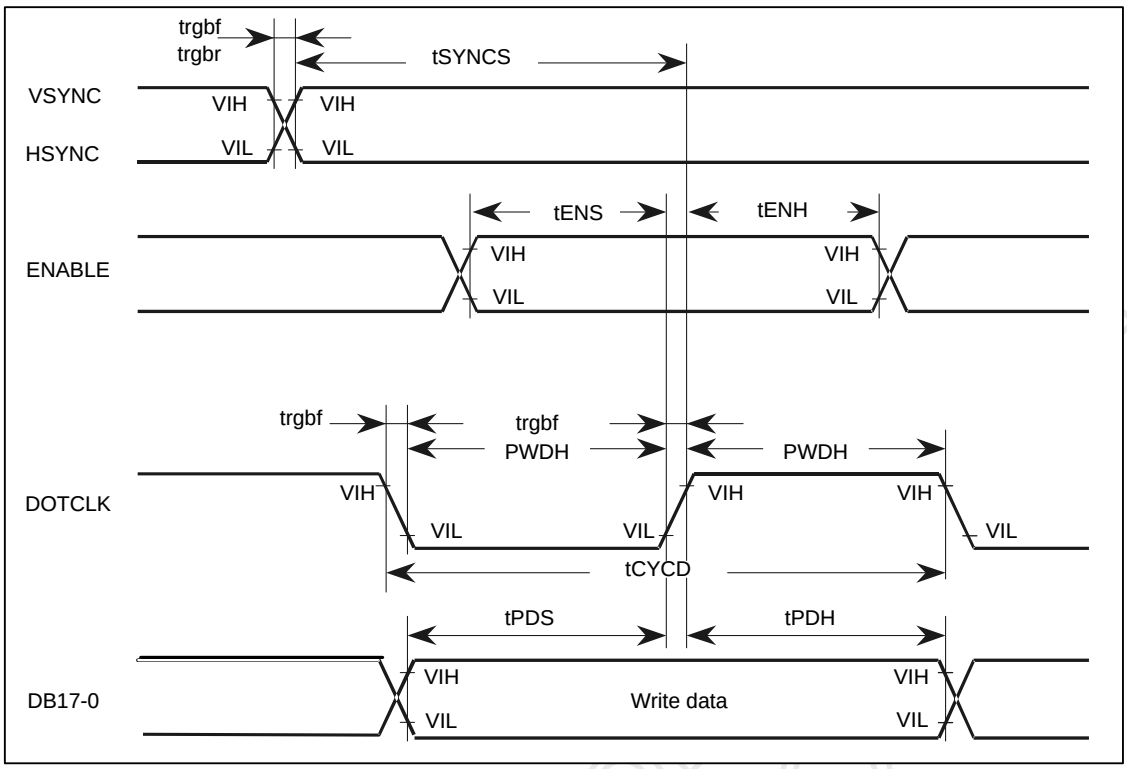


Figure 17. 4 RGB Interface Operation

LCD Driving Output

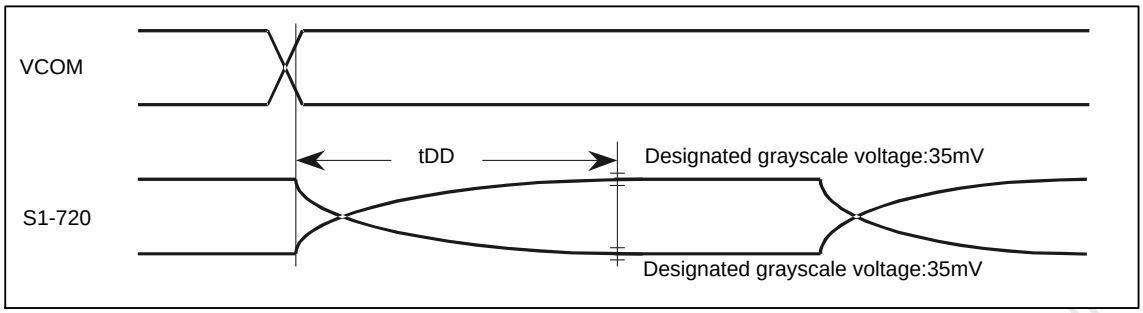


Figure 17. 5 LCD Driving Output

Reset Operation

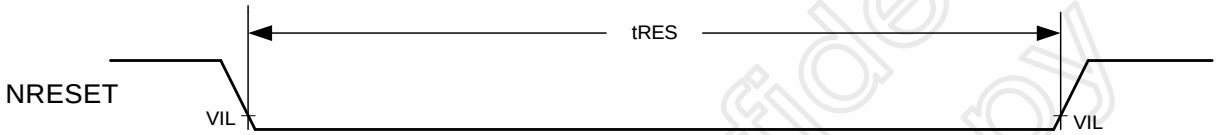


Figure 17. 6 Reset Timing

18. Ordering Information

Part NO.	Package
HX8312-A000PDxxx	PD: means COG xxx: means chip thickness (μm), default 400 μm

19. Revision History

Version	EFF.DATE	DESCRIPTION OF CHANGES
01	2005/05/06	New setup
02	2005/07/11	1. Add note in p.11. 2. Change Pin 216 ~ Pin 219 from VSSD to VSSD2 inp.11 and p.12. 3. RGB interface description and drawing correction in p.37 ~ p.45 4. Add “Please note that the value in R139 must be ≥ “20”h in p.49. 5. Add BGR bit function in p.50, p.51 and p.107. 6. Add “Inhibited to use” in p.52. 7. Delete note in p.53 8. Change note and setting value in example in p.55. 9. Change the color definition (Table.5.9) for PSEL bit setting in p.57. 10. Define SAW6-0 =”00h” in Table 6.2 as “setting inhibited” in p.59. 11. Delete WNRGB (D3 bit of R2) function in p.94. 12. Change: XVCOMG = 0 **à** VCOML level is decided by VCM and VDV bits in p.83 and p.98. 13. Change device ID default value to “0C”h in R50 in p.100.
	2005/08/23	1. Add the “Ordering Information” section, page 120.
03	2005/10/04	1. Delete “VDH pin description in p.11. 2. Correct the X address mapping in Table. 4.2 ~4.4 in p.51~ p.52. 3. Correct the width of chip from 1.670um to 1.670mm in p.18. 4. Correct the alignment mark circle diameter from 50um to 20um in p.19.
	2005/11/08	1. Add AC and DC characteristic parameter in p.108~p.119. 2. Redrawing the on/off flow in p.89 and p.90 3. Change the power on / off flow in p.87