

PRELIMINARY Product Brief



General Description:

iChipSecTM CO2128/48LI-3 is a full-featured programmable Internet Protocol (IP) Communication Controller chip that acts as a coprocessor to offload security and IP network connectivity tasks from any host processor. The IP ControllerTM is ideal for enabling devices to achieve secure, high-speed throughput and access to IP networks via 10/100BaseT or 802.11b/g wireless LANs, and cellular or dial-up modems. Typically only one manmonth is needed for hardware engineering and adding IP connectivity commands to the application.

The CO2128 firmware supports up to 10 simultaneous active TCP/UDP sockets and two listening sockets; HTTP, SMTP, MIME, POP3, FTP and Telnet clients; a Web/WAP server with two sites; and serial-to-IP bridging. Firmware flavors supporting different combinations of protocols and features will be available.

Security features include a random number generator, SHA-1/256 secure hash accelerator, AES-128/192/256 encryption accelerator, 3DES, SSL3/TLS1, and WEP/WPA2 encryption for WiFi.

iChipSec CO2128 uses an open software architecture that permits the user to select and program the firmware flavor that provides the Internet protocols and other features required for his application. CO2128 is shipped from the factory with a boot loader that accepts the customer-selected firmware flavor.

CO2128 stores the Internet protocol stack and Internet configuration parameters in the host's memory. The firmware can run from external flash or it may be loaded locally via RS-232, two-wire, SPI or USB interfaces. Firmware can be remotely updateable via sockets, FTP or the Web if external flash is used.

The chip includes a 32-bit ARM7TDMI RISC processor, 256KB SRAM, and a bus to access external memory or communication devices. The integrated boot loader enables the host to load the firmware via any of the included interfaces.

The CO2128 peripheral set includes a USB v2.0 full-speed host and device port; 10/100BaseT Ethernet MAC with MII and RMII; two USARTs; smart card, SPI, SSC, two-wire, and high-speed parallel interfaces; and one-channel 10-bit ADC.

CO2128 features several power-save modes for energy saving, and can shut down blocks not in use. It has an internal 1.2v LDO power supply. It comes in a 128-pin LQFP RoHS-compliant package and operates in the industrial temperature range.

iChipSec CO2128/48LI-3 IP Communication Controller

Key Features:

- Complete Internet Protocol stack
- 3DES, SHA-1/256, AES-128/192/256, SSL3 encryption
- UDP acceleration in hardware
- 10/100BaseT Ethernet MAC
- USB v2.0 full-speed host and device
- Many communication interfaces
- Smart card interface and 10-bit ADC

Internet Protocols:

- Basic Protocols: IP, UDP, TCP, PING, DNS, NTP, SSL3/TLS1, FTPS
- Modem firmware flavor: PPP, LCP, IPCP, PAP, CHAP, or script authentication
- LAN firmware flavor: ARP, ICMP, and DHCP
- Optional: SMTP, POP3, MIME, HTTP, FTP, Telnet, and WPA2 (according to firmware flavor)
- Optional Web/WAP server with two Web sites

Application Program Interface:

Connect One's AT+iTM protocol eliminates the need for Internet programming and minimizes changes to the host application, while the SerialNETTM serialto-IP bridging mode eliminates the need for any change to the host application. AT+i commands are intercepted by iChipSec, which puts the host device into Internet mode. AT commands pass transparently from the host processor to the communication peripheral without any intervention by iChipSec.

Hardware Description:

- Package: 128-pin LQFP, RoHS-compliant
- Dimensions: 14 x 20 x 1.4 mm, 0.5 mm pitch
- Core CPU: 32-bit RISC ARM7TDMI, 0.13 micron, low-leakage
- I/O Operating Range: 3.3v +/- 10%
- Core Operating Range: 1.2v +/- 10%
- Operating Frequency: Up to 48MHz
- Operating Humidity: 90% max. (non-condensing)
- Operating Temperature Range: -40° to 85° C (-40° to 185° F)
- Power Consumption with external VDD Core @ 1.2v: 190mW (typical), Sleep mode current: <200 uA
- Interfaces: Two USARTs, two-wire, two SPI, SSC, USB v2.0 host and device, external bus interface, high-speed parallel bus
- Includes 16-bit watchdog timer



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Block Diagram:



Mechanical Views:



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Pin-out:



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