The non-linear DSP Company

DATA SHEET

NV221

Progressive Scan Video Display Processor with Copy Protection

October, 2001
nDSP Corporation

Preliminary specification

nDSP reserves the right to make changes without further notice.

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1 General Description

NV221 is a high-quality, digital video display processor that incorporates nDSP's patented deinterlacing and video enhancement algorithms to convert standard interlaced video signals into progressive scan signals. The video algorithms are highly efficient and require only 2MB of low cost SDRAM. The chip combines a triple DAC, a memory controller, auto-configuration, Macrovision copy protection, CGMS and many other functions into a single device. This high level of integration enables simple, flexible, cost-effective solutions featuring fewer required components. The progressive output is suitable for display on LCD or DLP panels, or on progressively scanned CRT displays. The NV221 is well suited for progressive-scan DVD players, multimedia monitors, LCD TVs and progressive-scan CRT TVs.

2 Features

Deinterlace Processor
- Interlaced to progressive deinterlacer
  - NTSC to SDTV 480P
  - PAL to SDTV 480P/576P
- Per-pixel motion compensated deinterlacing algorithms to produce artifact-free progressive scan video signals
- Film mode for 3:2 pull down materials

Interlaced Video Input Options
- 60 Hz, 525-line (NTSC) signal
- 50 Hz, 625-line (PAL) signal
- ITU-R BT656 4:2:2 8-bit digital port

Video Input Formatter
- Input format detection
- Motion adaptive noise reduction
- Mode 2 master/slave operations supported
- Color space converter

Video Output Options
- Interlaced 480i/576i/1080i DTV signals
- Progressive 480P/576P/720P DTV signals
- VGA/SVGA/XGA @60Hz
- Analog video ports:
  - Component YPbPr with sync
  - Component RGB/YUV

Video Output Formatter
- Frame rate up conversion
  - 50 up to 75/100 Hz (PAL)
  - 60 up to 90/120 Hz (NTSC)
- Triple 10-bit digital-to-analog converter (DAC)
- Color space converters
- Selectable output color space: YUV or RGB

Video Enhancement
- DCTI/DLTI (Digital color/luminance transient improvement)
- Digital brightness, contrast, hue and saturation control
- Digital luminance peaking
- Black level expansion
- Independent x and y zoom
- Square / non-square pixel support
- On-board color bar generation

Copy Protection
- Macrovision anticopy facility (Version 7.1)
- CGMS (Copy Generation Management System)

System
- Built-in memory controller
- 2MB of x16 SDRAM as field memory
- I^2C-bus interface

Environmental
- Standard 100-pin PQFP package
- 3.3V power supply with 5V tolerant I/Os

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3 FUNCTIONAL BLOCK DIAGRAM

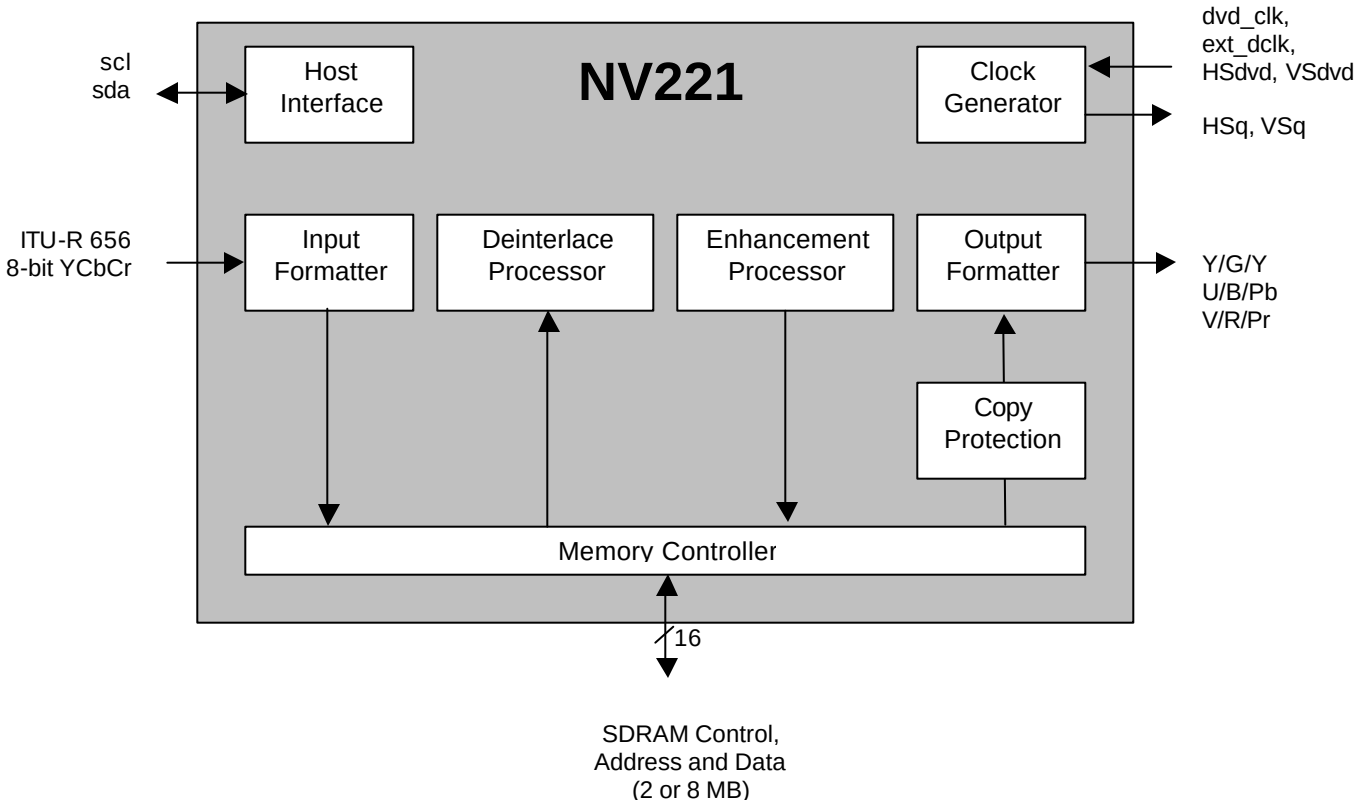


Figure 1. NV221 Block Diagram

4 ORDERING INFORMATION

PART NUMBER	PACKAGE	DESCRIPTION	VERSION
NV221	PQFP 100	Plastic quad flat package; 100 leads	1.0 Rev C

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5 PINNING INFORMATION

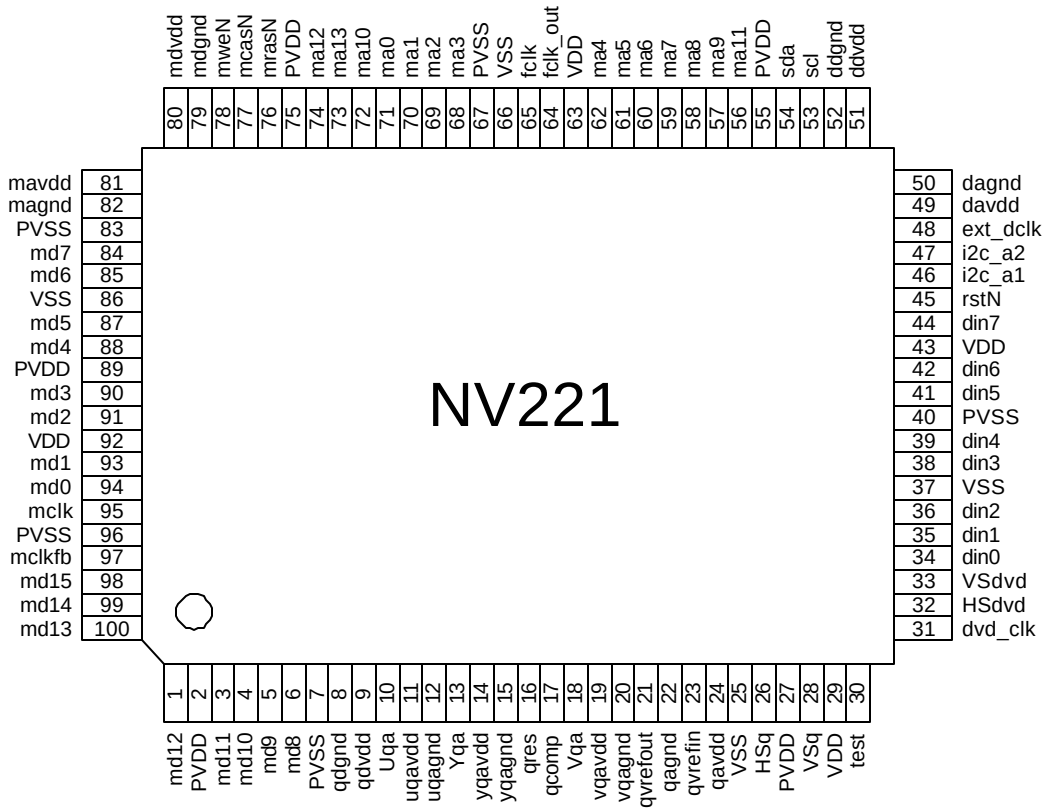


Figure 2. Pin Configuration

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5.1 Pin Description

Table 1. Digital Video Input

Pin Name	Pin Number	Type	Description
VSdvd	33	I/O	Vertical sync for all DVD modes.
HSdvd	32	I/O	Horizontal sync for all DVD modes.
dvd_clk	31	I	Video input clock (27MHz).
din[7:0]	44,42,41,39, 38,36,35,34	I	8-bit 4:2:2 multiplexed YCbCr pixel port (ITU-R 656). din0 represents the LSB.

Table 2. System Power

Pin Name	Pin Number	Type	Description
PVSS	7,40,67,83,96	G	Peripheral digital ground..
VSS	25,37,66,86	G	Core digital ground.
PVDD	2,27,55,75,89	P	Peripheral digital Vdd (3.3 V power supply)
VDD	29,43,63,92	P	Core digital Vdd (3.3 V power supply).

Table 3. Clock Generator

Pin Name	Pin Number	Type	Description
fclk	65	I	External crystal input for the fixed clock *fclk*. Connect to a 10 MHz crystal.
fclk_out	64	O	External crystal output for the fixed clock *fclk*. Connect to a 10 MHz crystal.
dagnd	50	G	Analog ground pin for the display clock PLL.
ddgnd	52	G	Digital guard ring and global ground pin for the display clock PLL.
magnd	82	G	Analog ground pin for the memory clock PLL.
mdgnd	79	G	Digital guard ring and global ground pin for the memory clock PLL.
davdd	49	P	Analog power pin for the display clock PLL.
ddvdd	51	P	Digital guard ring and global power pin for the display clock PLL.
mavdd	81	P	Analog power pin for the memory clock PLL.
mdvdd	80	P	Digital guard ring and global power pin for the memory clock PLL.
ext_dclk	48	I/O	External dclk.

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Table 4. System Interface

Pin Name	Pin Number	Type	Description
rstN	45	I	Asynchronous reset initializes the IC to a known state. Active low. Must be continuously asserted for a minimum of 100 µs after power-up to satisfy the SDRAM power-up requirement.
scl	53	I	Clock signal of I^2C bus (TTL pull-up)
sda	54	I/O	Data signal of I^2C bus (TTL pull-up)
test	30	I	Test mode enable. Active high.
i2c_a1	46	I	Programmable address bit 1 of I^2C bus.
i2c_a2	47	I	Programmable address bit 2 of I^2C bus.

Table 5. Memory Unit

Pin Name	Pin Number	Type	Description
ma[13:0]	73,74,56, 72,57,58, 59,60,61, 62,68,69, 70,71	O	Memory address bus. Multiplexed row and column address and bank select. Row addresses use *ma[11:0]* for 8MB SDRAM and *ma[10:0]* for 2MB SDRAM. Column addresses use *ma[7:0]*. Note that *ma[10*] is a control signal during column address charging and precharging. For 8MB SDRAM the bank select pins *ba0* and *ba1* should be connected to *ma[12]* and *ma[13]*, respectively; for 2MB SDRAM, *ba0* to *ma[12]* only
mcasN	77	O	Column address strobe latches column addresses on the positive edge of *mclk* when low.
mclk	95	O	Memory clock.
mclkfb	97	I	Memory clock feedback. For latching in read data.
md[15:0]	98,99,100, 1,3,4,5,6, 84,85,87, 88,90,91, 93,94	I/O	Memory data bus.
mrasN	76	O	Row address strobe. Latches row addresses on the positive edge of *mclk* with *mrasN* low
mweN	78	O	Memory write enable. Enables write operation and row precharge. Latches data in starting from *casN* and *mweN* low

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Table 6. Analog Video Output

Pin Name	Pin Number	Type	Description
Yqa	13	O	Analog component video Y/G/Y output.
Uqa	10	O	Analog component video U/B/Pb output.
Vqa	18	O	Analog component video V/R/Pr output.
qcomp	17	I/O	Compensation pin. This pin should be connected through 0.1uF ceramic capacitor to *qavdd* (+3.3v) externally.
qvrefin	23	I	Reference voltage input.
qvrefout	21	O	Voltage reference output. This output nominally delivers 1.2824v reference voltage from bandgap reference block. It is normally connected to *qvrefin* pin.
qres	16	I/O	Full-Scale adjust resistor. A resistor should be connected between this pin and qagnd to control the magnitude of the full-scale video signal. *qres*(ohm)=*qvrefin*(V)*2.484/IOFS(A), where IOFS is full-scale output current.
qagnd	22	G	Analog ground pin.
yqagnd	15	G	Analog ground pin for Y channel.
uqagnd	12	G	Analog ground pin for U channel.
vqagnd	20	G	Analog ground pin for V channel.
qavdd	24	P	Analog power supply (+3.3V).
yqavdd	14	P	Analog power pin (+3.3V) for Y channel.
uqavdd	11	P	Analog power pin (+3.3V) for U channel.
vqavdd	19	P	Analog power pin (+3.3V) for V channel.
qdgnd	8	G	Digital ground pin.
qdvdd	9	P	Digital power supply (+3.3V).
HSq	26	O	Horizontal sync output.
VSq	28	O	Vertical sync output.

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6 SYSTEM DESCRIPTION

6.1 Video Input Unit

The NV221 video display processor is intended to interface to off-the-shelf video and MPEG decoders. As a consequence the NV221 accepts 4:2:2 YCbCr pixel data via an ITU-R 656 8-bit parallel pixel port at a 13.5 MHz data rate. Y has a range of 16 to 235, Cb and Cr have a range of 128 ±112. This 4:2:2 data stream is interpolated into 4:4:4 component video (YUV) and the resultant YUV video runs at a rate of 27 MHz.

The NV221 requires a video input clock of 27 MHz for standard operation. The output video frames are synchronized with the incoming timing reference codes. Alternatively the NV221 accepts (and can generate) horizontal sync and field timing signals.

The Video Input Formatter includes motion detection and noise reduction.

6.1.1 Video Input Formatter

The Video Input Formatter is able to automatically detect the input format according to the total number of lines sampled between vertical syncs. The total includes both blanking and active lines. The NV221 supports NTSC and PAL standards.

The format detection is enabled whenever the *detect_form* 0x2A[3] bit is set to 1. The detected format is reported in the corresponding *input_format* 0x28[4:2] field. Alternately, one of the standard formats may be requested, by turning off the *detect_form* bit and programming the *input_format* field.

Once the format is known, the framing of the input signal may begin. The framing parameters consist of an active region offset and resolution. The active region offset refers to the vertical and horizontal blanking intervals and are specific to each input format. The input resolution refers to the active region dimensions of the input video signal. Table 7 shows the various default resolutions and offsets for NTSC and PAL. The height of the even field is given in the case of interlaced modes; the height of the odd field is always assumed to be one line larger. The default vertical offset is identical for both the odd and even fields.

The user may override the default resolution and offsets for the input format. The default offsets are overridden by setting the *offset* 0x2A[0] bit and programming the *hsta, odd_vsta*, and *even_vsta* fields in registers 0x2B to 0x2D.

Table 7. Default Active Region Resolutions and Offsets

Input Format	Width	Height	Vertical Offset	Horizontal Offset
NTSC	720	240	16	122
PAL	720	288	22	132

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Table 8. Programming and Detecting the Active Region Size

detect_form	Width	Height	*input_format*
0	Default resolution according to Table 7		Specified format (R/W)
1	Default resolution according to Table 7		Detected format (RO)

6.1.2 DVD Modes

The NV221 has several video timing modes of operation that allow it to be configured as either system master video timing generator or a slave to the system video timing generator. Mode 2 (master and slave options) is supported. The specific DVD mode is specified by programming the *dvd_mode* 0x29[5:4] field.

Mode 2 (ITU-R 656), Slave Option
The NV221 accepts horizontal and vertical sync signals. A coincident low transition of both HSdvd and VSdvd inputs indicates the start of an odd field. A VSdvd low transition when HSdvd is high indicates the start of an even field.

Mode2 (ITU-R 656), Master Option
The NV221 can generate horizontal and vertical sync signals. A coincident low transition of both HSdvd and VSdvd inputs indicates the start of an odd field. A VSdvd low transition when HSdvd is high indicates the start of an even field.

6.1.3 Noise Reduction Filters

Figure 3 shows a block diagram of the motion adaptive noise reduction. The structure of the motion adaptive noise reduction is identical for the luminance signal and chrominance signals. The motion detector generates motion levels from input video data and field memory data. The input video data may be low-pass filtered with a FIR filter before being analyzed by the motion detector.

Parameters: *kimdet0, kimdet1, kimdet2*
Value range: 0…31
Default value: *kimdet0 = 6*
kimdet1 = 4
kimdet2 = 1

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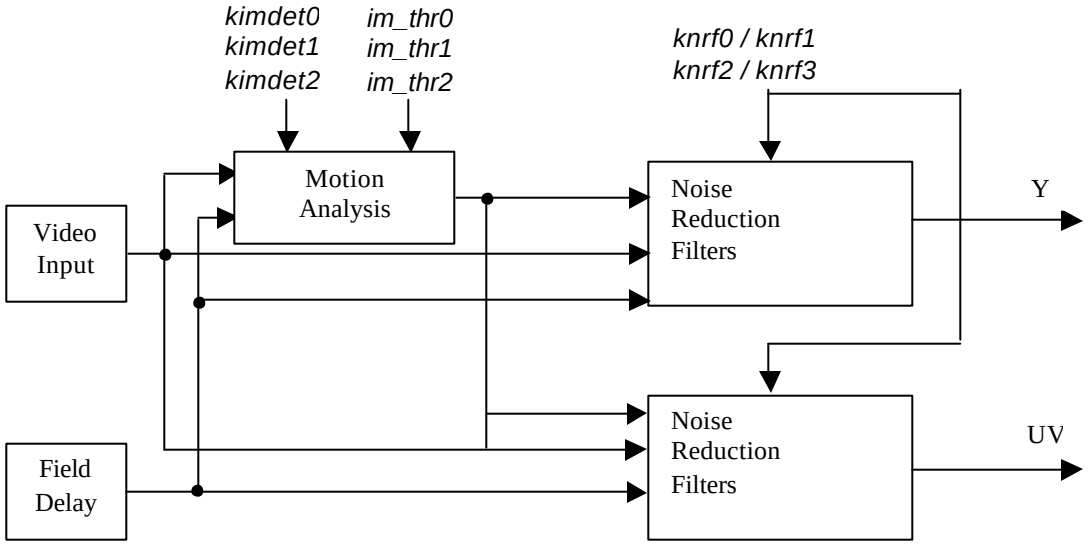


Figure 3. Motion Adaptive Noise Reduction Filters

A set of parameters defined by registers *im_thr0, im_thr1,* and *im_thr2,* set thresholds on the motion level. These divide the range of motion (from no motion to maximum motion) into four zones.

Parameters: *im_thr0, im_thr1, im_thr2*
Value range: 0…255
Default value: *im_thr0* = 3
im_thr1 = 6
im_thr2 = 10
Properties:
$0 \le im_thr0 < im_thr1 < im_thr2 \le 255$

Based on the motion level present, one of four noise reduction filters is selected. Registers *knrf0, knrf1, knrf2,* and *knrf3* can program parameters controlling these motion adaptive noise reduction filters. The parameters control the amount of noise filtering used in each motion zone.

Parameters: *knrf0, knrf1, knrf2, knrf3*
Value range: 0…128
Default value: *knrf0* = 64
knrf1 = 84
knrf2 = 104
knrf3 = 128
Properties:
$0 \le knrf0 < knrf1 < knrf2 < knrf3 \le 128$

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6.2 Memory Controller

The integrated memory controller takes care of addressing and control of the external SDRAM. The SDRAM should have LVTTL-compatible inputs and outputs.

The SDRAM types used with the NV221 should be organized as 1Mx16, each bank having 4096 pages of 256 words of 16 bits. A typical configuration uses one 16Mb (1Mx16) or 64Mb (4Mx16) SDRAM with a 16-bit data bus, allowing for 2MB or 8MB of storage. The target SDRAM types are Hyundai HY57V161610D (2MB) and Micron MT48LC4m16A2 or Hyundai HY57V641620HGT (8MB) or other compatible devices.

Due to memory communication requirements this memory interface runs at 81 MHz. The size of position of the video input buffer is programmable. By default, 2MB of storage is required for NTSC and 4MB of storage is required for PAL.

6.2.1 Frame Buffer Operations

The memory controller controls the flow of data between the NV221 and either 2 or 8 MB of external 16-bit SDRAM. The essential function is to operate the SDRAM as a frame buffer between the input and display units.

Data arrives at the frame buffer either in *video* or *motion* formats from the input unit or in raw form from the host interface via the I^2C-bus. Interlaced data arrives as separate 16-bit 4:2:2 video and 4-bit motion components stored in different regions of the SDRAM. Similarly, data exits the memory unit either in video or motion formats to the display unit or in raw form to the host interface. The video data is also fed back to the input unit.

On the input side, the most recent four fields – two odd and two even – are stored in the frame buffer. *Freeze* and *step* functions may be employed for the rejection of all or a fixed ratio of incoming fields. When in freeze mode, the entire frame buffer or a portion thereof may be *painted* a solid background color or, for diagnostics, a two-dimensional color bar pattern.

The active input region stored in the frame buffer is defined by the coordinates of its width *i2m_hlen* 0x40[6:0] and height *i2m_vlen* 0x41[7:0] and its top left corner *i2m_left* 0x44[6:0] and *i2m_top* 0x45[7:0]. When *i2m_siz* 0x40[7] = 0 and *i2m_offset* 0x44[7] = 0, there is no offset from the upper left origin and the size of the active input region follows Table 7.

On the output side, a set of line buffers is presented to the display unit from the merging of the most recently stored odd and even fields. In this operation, 5 line buffers of 16-bit 4:2:2 video plus 4-bit motion are used. The merging of the odd and even fields can be either straight deinterlaced or inverse 3:2 pulldown, depending on whether *film mode* has been detected.

The active display region is defined by the coordinates of its width *m2d_hlen* 0x5C[6:0] and height *m2d_vlen* 0x5D[7:0] and its top left corner *m2d_left* 0x58[6:0] and *m2d_top* 0x59[7:0]. When *m2d_siz* 0x5C[7] = 0 and *m2d_offset* 0x58[7] = 0, there is no offset from the upper left origin and the size of the active display region follows Table 7.

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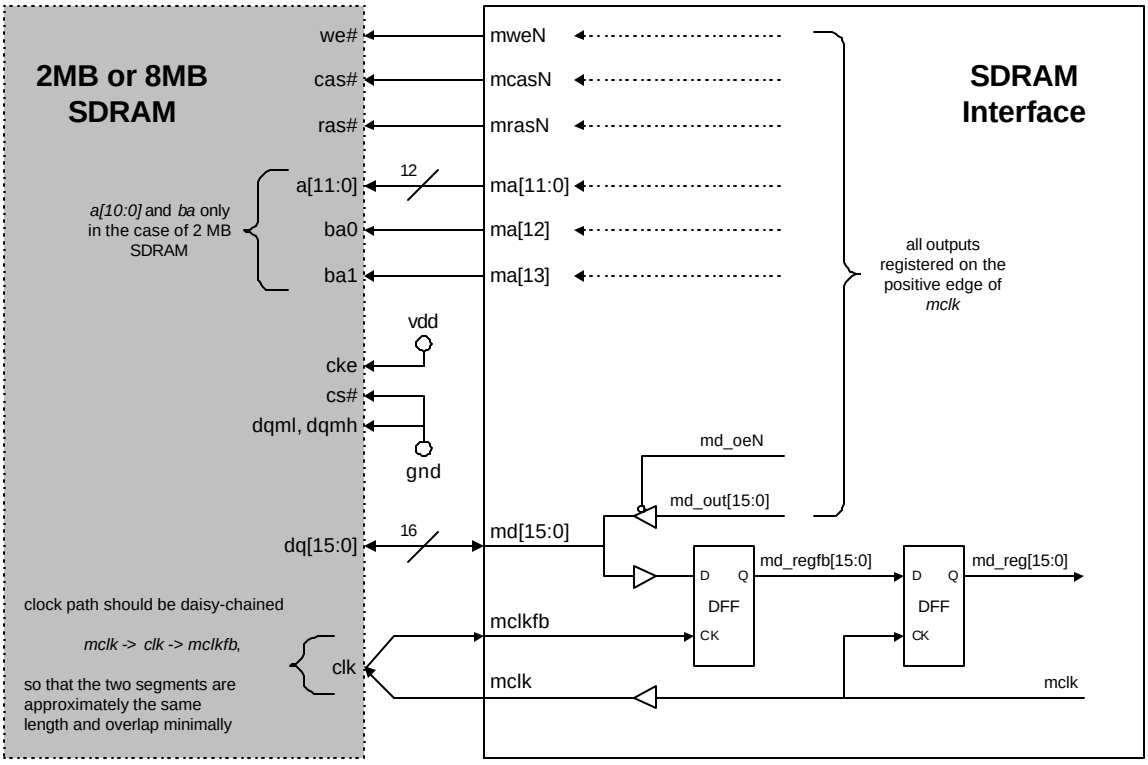


Figure 4. SDRAM Interface Block Diagram

6.2.2 SDRAM Interface

Upon reset, the memory controller will generate the necessary commands to initialize the memory before servicing memory requests from the NV221. The reset pin rstN must be asserted for at least 100 µs following power-up to satisfy the initialization requirements of the SDRAM.

Figure 4 shows a block diagram of the SDRAM interface. All outputs from the SDRAM interfaced are registered on the positive edge of *mclk*. The clock path should be daisy-chained

mclk -> clk -> mclkfb

so that the two segments are approximately the same length and overlap minimally. In the case of 2MB SDRAM, only memory address bus ma[10:0] and ma[12] bits are used to interface with the SDRAM address inputs a[10:0] and bank address input ba. For the 8MB SDRAM usage, ma[11:0] should be connected to a[11:0]; ma[12] and ma[13] should be tied to ba0 and ba1, respectively.

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6.2.3 Memory Refresh

Typically an SDRAM part requires refreshing at an average interval of every 15.625 µs. While in general it is good to set the refresh interval *ref_len* 0x57[1:0] to as large a number as possible to optimize bandwidth, a certain maximum setting is required depending on the speed of the memory clock *mclk*. Refer to the following table for the optimal (maximum) setting. The minimum *mclk* frequency supported is 10 MHz.

Table 9. Maximum Refresh Interval Settings

Frequency Range *mclk*	Maximum Refresh Interval *ref_len*
10 – 50 MHz	0
51 – 80 MHz	1
81 – 110 MHz	2
> 110 MHz	3

6.3 Display Unit

6.3.1 Display Timing

Table 10. Default Output Sync Timing

Format	hsp	hbp	hap	vsp	vbp	vap
NTSC	64	72	720	2	26	496
PAL		76				472

6.3.2 Deinterlace Processor

The de-interlacing processor converts multiple interlaced video fields into a progressive video frame based on 3D motion compensation and non-linear interpolation algorithms. The NV221 supports 3 modes of deinterlacing: simple, vertical interpolation and angle interpolation. In the simple mode, (*di_bypass* 0x70[2] is set to 1), the interlaced video is deinterlaced without undergoing vertical or angle interpolation. For better edge rendition, field interpolation can be deployed in the vertical or angular direction. These modes are programmed by setting *di_bypass* to 0 and *vert_interp* 0x70[1] to 0 (angle interpolation mode) or 1 (vertical interpolation mode).

6.3.3 Upscaler

The upscaler remaps an incoming *m*-column by *n*-row frame into an outgoing *p* by *q* frame. The incoming horizontal length *m* is determined according to *m2d_siz* 0x5C[7] and *m2d_hlen* 0x5C[6:0] fields. Similarly, the upscaler determines the incoming vertical length n is by examining the *m2d_siz* and *m2d_vlen* 0x5D[7:0] fields.

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Table 11. Default Output Resolutions by Display Mode

us_mode	Format	Width (*hlen*)	Height (*vlen*)
0	NTSC/480i/480p	720	480
1	PAL	720	576

The outgoing horizontal and vertical lengths, p and q, are also programmable. Table 11 shows the default output resolutions, which can be programmed by setting *us_remap* 0x71[0] to 1 and selecting the output resolutions using *us_mode* 0x71[3:1]. Alternatively, the upscaler can resize the picture to any arbitrary size *(us_hlen* by *us_vlen)* when *us_size* is set to 1. The upscaler can be turned off by setting *us_size* and *us_remap* to 0.

6.3.4 Video Enhancement

The Video Enhancer block contains the following key functions: Y-Peaking, DLTI, DCTI, Brightness and Contrast, Hue and Saturation, and Black Level Expansion. These functions are discussed in detail below.

Y-Peaking Filter

The peaking filter improves the overall frequency response of the luma signal. There are three filters applied to the luma signal: high-pass filter, band-pass filter, and low-pass filter. The outputs of these filters are weighted by gain factors and summed together. The gain factors are separately programmable through registers *khpw* 0xD0[4:0], *kbpw* 0xD1[4:0] and *klp* 0xD2[2:0]. Coring is added to obtain no gain for low amplitudes in the (high-pass + band-pass) signal, which is considered to be noise. Coring levels can be programmed via the *peaking_coring* 0xD3 register.

DLTI & DCTI

The Digital Luminance Transient Improvement (DLTI) and Digital Color Transient Improvement (DCTI) are intended to enhance video by replacing the edges of the video with edges that have steeper rise and fall times. DLTI and DCTI are different from peaking in that they do not increase the peak-to-peak video at its output; rather it turns sloped or sinusoidal waveforms into rectangular or square waveforms with the same duty cycles and peak-to-peak amplitude.

The NV221 can perform a coring function, in which it forces all values below a programmed threshold level to be 0. This is useful to enhance immunity against nose. Via the configuration registers (0xD4 and 0xD5) it is possible to control: DLTI gain width, DLTI coring threshold, DCTI gain width, DCTI coring threshold, and selection of simple, or improved first differentiating DCTI filter.

Brightness and Contrast

Programmable brightness and contrast are used to compensate for poor video sources. Contrast is adjusted by multiplying the luminance data (after sync and blank information have been removed) by a constant, *contrast* 0xD6[5:0]. The video enhancement module can also adjust brightness by adding or subtracting a constant, *brightness* 0xD7[7:0], from the luma value. The brightness adjustment is done after the contrast adjustment to avoid introducing a varying DC offset due when adjusting the contrast.

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Hue and Saturation

Hue refers to the wavelength of the color and is used to describe base color- red, green, yellow, etc. Saturation is the amount of color present. For example, a lightly saturated red looks pink. The hue and saturation algorithm uses the *hue* 0xD8[7:0] and *saturation* 0xD9[7:0] fields.

Black Level Expansion

Black level expansion (BLE) enhances the contrast of the picture. The dark regions of the picture are changed to black, while bright areas remain unchanged. The advantage of this black-level expansion is that the black expansion is performed only if it will be noticeable to the viewer. The BLE works adaptively. Above a value programmed by the threshold value *ble_thr* 0xDF[7:0], there is no black expansion. Below this point all luminance values are adjusted according to:

$$Y_{out} = Y_{in} + (Y_{in} - ble_thr * 4) * ble_gain / 32.$$

Color Space Conversion

Color space conversion uses *prim_cs* 0x78[4:3] and *common_cs* 0x78[2:0] fields. The input primary channel color space is entered with *prim_cs* and the output common color space is specified with *common_cs*.

Table 12. Input Color Space

prim_cs	**Description**
0	YCbCr (601).
1-2	Reserved.
3	TV RGB (16..235 range).

Table 13. Common Output Color Space

common_cs	**Description**
0	YCbCr (601).
1	Y,-Cb, -Cr.
2-4	Reserved.
5	TV RGB (16..235 range).
6-7	Reserved.

Table 14. Supported Color Space Conversions

Input	**Output**		
	YCbCr	**Y,-Cb, -Cr**	**TV RGB**
YCbCr	Bypass	Yes	Yes
TV RGB	Yes	No	Bypass

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Blanking

Blanking sets YCbCr or RGB to fixed values during vertical and horizontal blanking. The blank value for Y can be selected to be either 0 or 64 using the *y_blank* 0x79[6] field. U and V are fixed to 512 in either case. In the case of RGB, blanking switches all three signals to 0. There is no bypass of the blanking algorithm.

Blue Screen

Blue screen sets active YUV or RGB to certain programmable values when the *blue_screen* 0x78[6] bit = 1. Configuration registers *blue_screen*, *y_blue* (0x79), *u_blue* (0x7A), and *v_blue* (0x7B) are used to specify the values according to:.

Y' = *{y_blue, y_blue[7:6]}*
U' = *{u_blue, u_blue[7:6]}*
V' = *{v_blue, v_blue[7:6]}*

The blue screen algorithm is turned off when *blue_screen* = 0.

6.3.5 Film Mode

The NV221 supports Film Mode whereby 3:2 pull-down sequences are detected and the frames remapped to support 60Hz progressive. A block diagram of Film Mode is shown in Figure 5.
The Film Mode Detect module detects the 3:2 pull-down sequences by examining the input video. The Memory Controller receives appropriate command to map the frames to support 60Hz progressive video in Memory, prior to deinterlacing. If no 3:2 sequences are detected, the video stream is stored in Memory without further processing.

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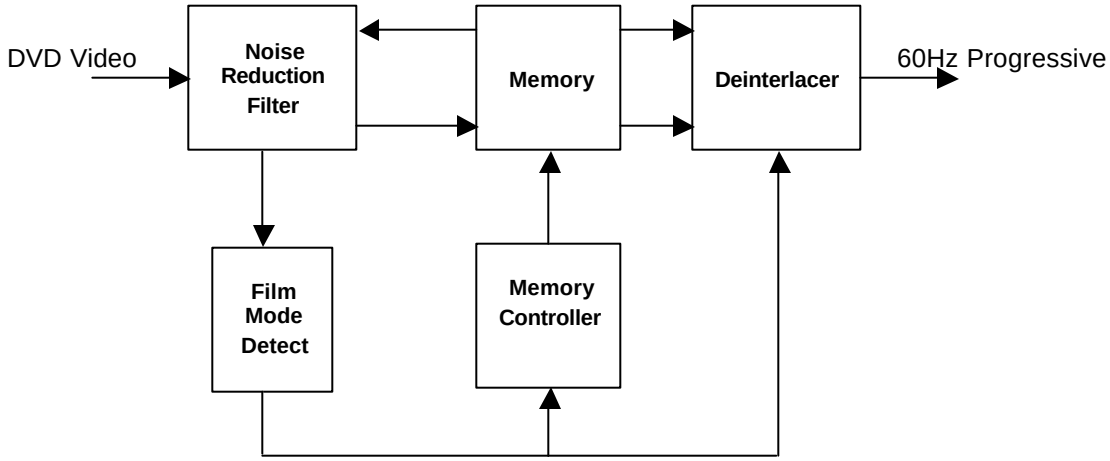


Figure 5. Film Mode Block Diagram

6.4 Analog Back-End

The analog back-end (ABE) generates analog RGB, YUV or YPbPr with triple 10-bit digital-to-analog converters (DACs). The analog RGB or YUV output is generated in synchronization with timing signals.

Conversion from digital to analog is separate for Y, U and V. Each converter uses an external resistor of approximately 75 ohms, connected between output and ground, to interface with low impedance output buffers.

Each digital-to-analog converter has its own supply and ground pins which are used for decoupling. An internal reference voltage of 1.23V is generated for each DAC. A compensation capacitor is connected to the *qcomp* pin and is assumed to be 0.5uF. A resistor of 147 ohms is connected to the *qres* pin and is used to set the reference current on the DACs.

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6.5 Copy Protection

The anticopy process is implemented according to the Macrovision version 7.1L1 specification developed by Macrovision Corporation, Sunnyvale, California. All luminance and chrominance signals include the Macrovision Anticopy Process. The NV221 incorporates an anticopy process technology that is protected by U.S. patents and other intellectual property rights.

The anticopy process is licensed for noncommercial, home use only. Reverse engineering or disassembly is prohibited. nDSP Corporation can only ship NV221 to customers licensed by Macrovision. A NV221 Macrovision supplement may be obtained, by Macrovision licensees, by contacting nDSP Corporation.

The component video interface with Macrovision (CVIM) is designed to meet standards of EIA-770.2-A and Specification of the Macrovision AGC copy protection waveforms for DVD applications with 525 (480P) progressive outputs. The copy protection module also supports placing the CGMS (Copy Generation Management System) into Y channel of the output data stream.

The copy protection module accepts progressive scan video inputs and generates outputs to meet the EIA-770.2 standard. The inputs are 30-bit YCbCr 4:4:4 data, Vsync, and Hsync. The output format is progressive scan 30-bit YCbCr 4:4:4 data with the embedded sync. Figure 6 shows a functional block diagram of the copy protection module.

6.5.1 Sync Signal Insertion

The sync signal is inserted into digital video signal (Y channel) prior to digital to analog conversion for allowing ease of use. Prior to the sync insertion, the active video data is shifted from 0 to Blanking Level (306). The mapped video data will then swing between the Y Blanking Level and 1023, while the range from 0 to Blanking will be used for sync insertion only. The sync insertion conforms to the timing requirement of EIA-770-2A. Figure 8 shows the insertion of sync signal. The video data mapping uses the following gain control formula.

Multiplier = (Output Max.- Output Blank)/Input Max.
Adder = Output Blank

6.5.2 CGMS

The NV221 places the CGMS (Copy Generation Management System) into Y channel of the output data stream. The CGMS generator is programmable and supports different standards. Both the American Standard EIA-805 and the Japanese Standard EIAJ CPR-1204 are supported.

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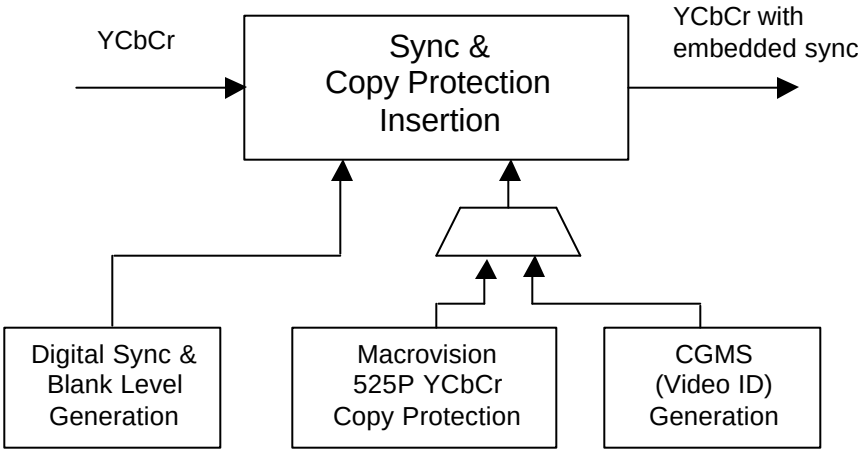


Figure 6. Copy Protection Block Diagram

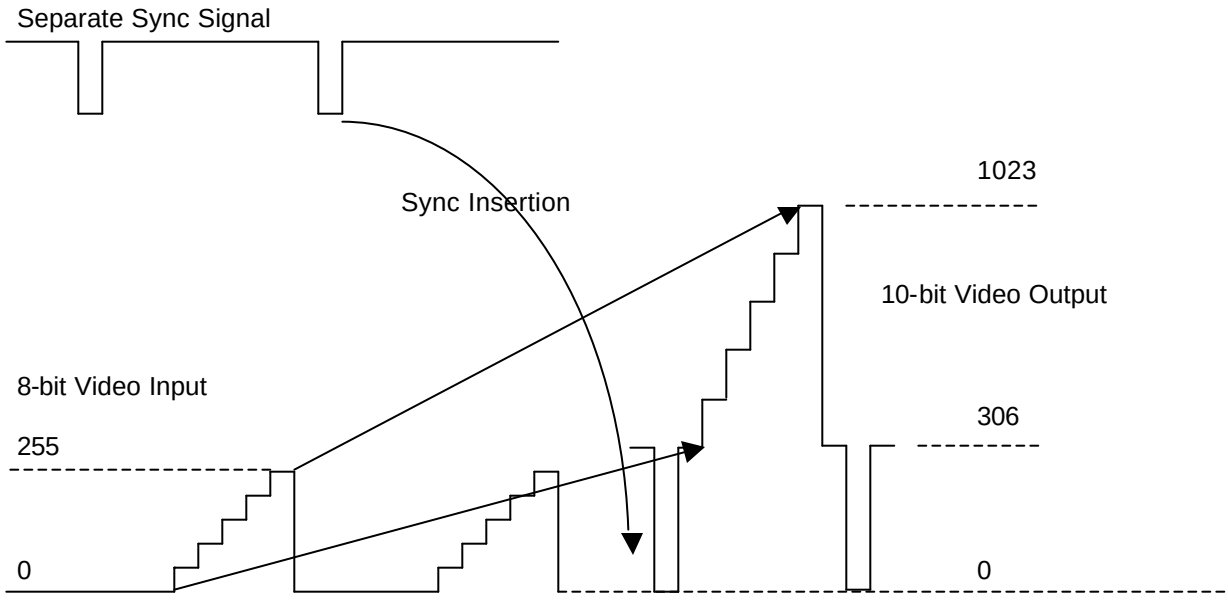


Figure 7. Mapping and Sync Insertion

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6.6 I²C Bus Description

The host interface provides programmable control capability to allow adjustment, calibration, and intelligent control of each subsystem. The NV221 provides this capability via the I²C bus. The I²C bus is a bi-directional, two-wire serial bus, consisting of a serial data line (SDA) and a serial clock line (SCL). The I²C-bus interface is used in slave receive and transmit mode for communication with a system microprocessor. The standardized bus frequencies of both 100 kHz and 400 kHz are supported. The 400 kHz (Fast Mode) requires 50ns glitch filters for both positive and negative glitches.

6.6.1 I²C Bus Protocol

Four I²C slave addresses (0110000, 0110010, 0110100 and 0110110) are reserved for NV221. The least significant bit of the slave addresses is fixed to zero. The next two least significant bits are configurable and can be defined by the level tied at their inputs *i2c_a1* (pin 46) and *i2c_a2* (pin 47).

The I²C-bus protocol is shown in Figure 9. All communications are initiated with a start condition (S) from the I²C-bus master, which is followed by the desired slave address and read/write bit.

In the WRITE mode (indicated by setting the read/write bit LOW), one sub-address follows the slave address acknowledgement. After the sub-address, a series of data bytes may follow. After the last data byte has been acknowledged, the I²C-bus master issues a stop condition (P).

In the READ mode (indicated by setting the read/write bit LOW), two transactions are required on the I²C control bus. The first transaction resembles a write operation with no data transfer. This step will write the desired sub-address into the internal address pointer. The next transaction reads one or more bytes from the NV221 starting from the sub-address set in the first transaction. The first byte of this transaction is the IC address with the read bit set. The second and subsequent bytes, if any, are read data from the NV221. The last byte is signaled by the I²C control master when it returns a “not acknowledge” for a data byte transmitted by the NV221.

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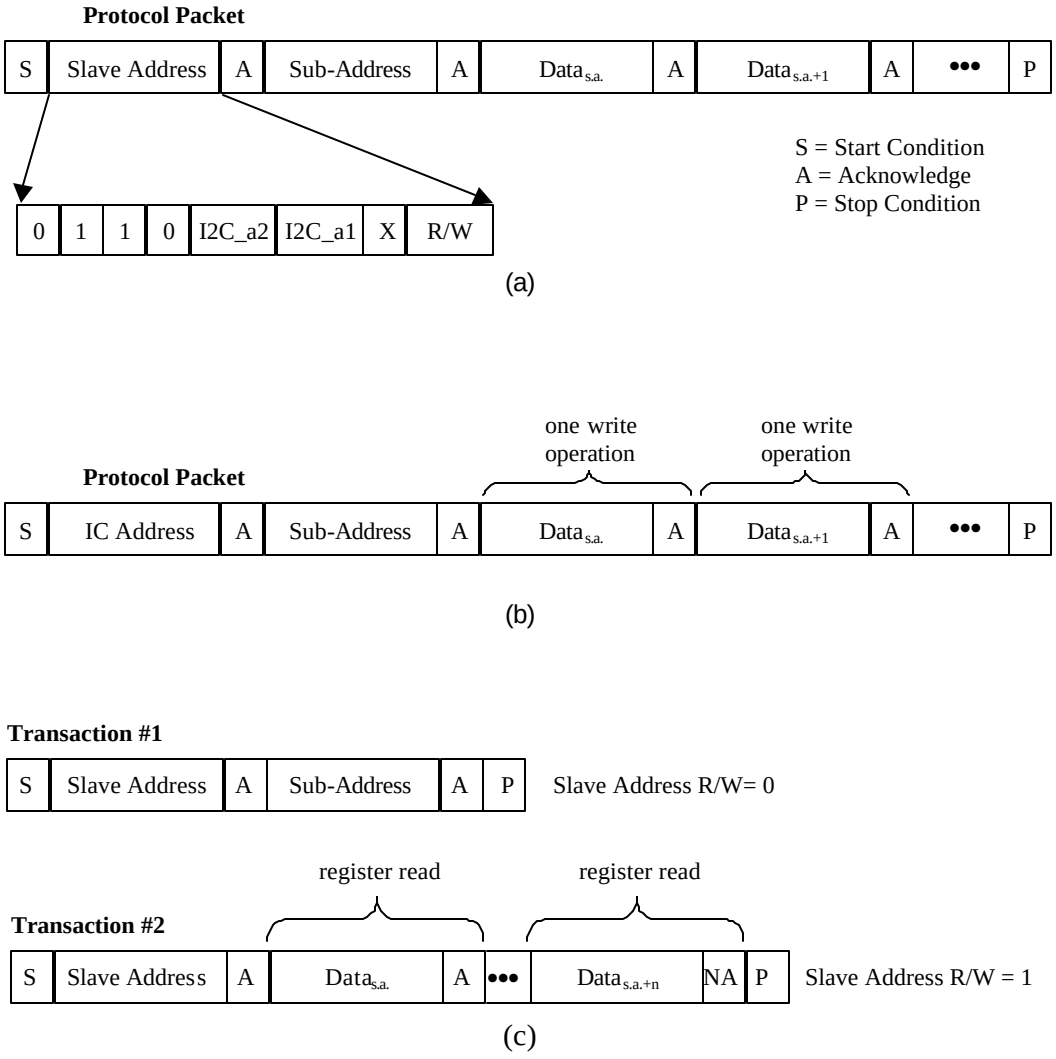


Figure 8. I²C-bus protocol. (a) Slave address; (b) I²C-bus WRITE mode; (c) I²C-bus READ mode.

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7 Configuration Registers

The NV221 register set is mapped into the 256-byte sub-address of the I²C interface. The sub-address assignment for each subsystem is given in the table above. All unlisted sub-addresses are reserved

Table 15. Register Mapping Overview

Sub-Address	Table	Sub-System
0x28 – 0x33 0xA0 – 0xA9	16	Input Control
0x40 – 0x5D	17	Memory Control
0x60 – 0x7F 0x98 – 0x9E 0xD0 – 0xEF	18	Display Control
0x10 – 0x14 0x90 – 0x97	19	System Control

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Table 16. Input Related Control

Sub-Addr	Bits	Default	Name	Description
0x28				
	5	0b	*video_err*	Video input error. Can be cleared only by a hard or soft reset. Read only. *video_err* = 0: no error *video_err* = 1: improperly framed video data.
	4:2	0h	*input_format*	When *detect_form* 0x2A[3] = 1, use *input_format* to specify the video input format. *input_format* = 0: NTSC *input_format* = 2: PAL. Otherwise, input *format* reports the format detected and is read only.
	1:0	0h	*input_type*	Video input type. Must be set to 0.
0x29				
	5:4	2h	*dvd_mode*	DVD timing modes of operation. *dvd_mode* = 2: slave option of DVD mode 2 *dvd_mode* = 3: master option of DVD mode 2
	3:2	2h	*uv_encode*	Encoding for UV components. *uv_encode* / Description 00 – 1's complement numbers. 01 – 2's complement numbers. 10 – positive binary numbers. 11 – Reserved.
	1	0b	*clk_del*	Clock delay adjustment. *clk_del* = 0: no delay *clk_del* = 1: one clock delay, effectively reversing the luma and chroma values.
	0	0b	*clk_edge*	Clock edge adjustment. *clk_edge* = 0: sample data on the rising edge of dvd_clk. *clk_edge* = 1: sample data on the falling edge.
0x2A				
	6	0b	*hsdvd_pol*	Polarity of *HSdvd* pin. *hsdvd_pol* = 0: active high *hsdvd_pol* = 1: active low.
	5	0b	*vsdvd_pol*	Polarity of *VSdvd* pin. *vsdvd_pol* = 0: active high *vsdvd_pol* = 1: active low
	4	1b	*422_conv*	Method for converting from 4:1:1 to 4:2:2 or from 4:2:2 to 4:4:4 formats. *422_conv* = 0: copy the UV sample *422_conv* = 1: bilinear interpolation
	3	1b	*detect_form*	Format detection enable on video data. *detect_form* = 0: input format is specified via *input_format* *detect_form* = 1: automatic format detection

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Table 16. Input Related Control *(Continued)*

Sub-Addr	Bits	Default	Name	Description
0x2A				
	0	0b	*offset*	Program enable for the top left corner of the active region via the *hsta* (0x2B[7:0], 0x2C[0]), *odd_vsta* 0x2C[7:1], and *even_vsta* 0x2D[7:0] fields. *offset* = 0: offset defaults according to Table 7. *offset* = 1: programmable offset values
0x2B				
	7:0	7Ah	*hsta[7:0]*	Lower 8 bits of starting pixel relative to the horizontal sync for active video. Valid only when *offset* 0x2A[0] = 1. Starting pixel = *hsta* pixels from horizontal sync
0x2C				
	7:1	10h	*odd_vsta*	Starting line relative to the vertical sync for an active odd video field. Valid only when *offset* 0x2A[0] = 1. Starting line = *odd_vsta* lines from vertical sync.
	0	0b	*hsta[8]*	Most significant bit (MSB) of starting pixel relative to the horizontal sync for active video. See 0x2B.
0x2D				
	6:0	10h	*even_vsta*	Starting line relative to the vertical sync for an active even video field. Valid only when *offset* 0x2A[0] = 1. Starting line = *even_vsta* lines from vertical sync.
0x30				
	1	1b	*il_srstN_fb*	Software reset echo (*feedback*) for the input unit. Can be used to detect the absence of a clock in the input unit. Read only.
	0	1b	*srstN*	Software reset. *srstN* = 0: reset the video input block. *srstN* = 1: resume operation.

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Table 16. Input Related Control *(Continued)*

Sub-Addr	Bits	Default	Name	Description
0x33				
	2	1b	*mn_testN*	Motion and noise test enable. Active low.
	1	1b	*mn_chroma*	Chroma enable. *mn_chroma* = 0: use luma values only *mn_chroma* = 1: include chroma in the calculation of motion detection and noise reduction
	0	0b	*mn_bypass*	Motion and noise bypass enable. *mn_bypass* = 0: no bypass *mn_bypass* = 1: bypass
0xA0				
	7:0	3h	*im_thr0*	Input motion threshold 0.
0xA1				
	7:0	6h	*im_thr1*	Input motion threshold 1.
0xA2				
	7:0	Ah	*im_thr2*	Input motion threshold 2.
0xA3				
	7:0	40h	*knrf0*	Noise filtering constant when the motion vector is in region 0.
0xA4				
	7:0	54h	*knrf1*	Noise filtering constant when the motion vector is in region 1.
0xA5				
	7:0	68h	*knrf2*	Noise filtering constant when the motion vector is in region 2.
0xA6				
	7:0	80h	*knrf3*	Noise filtering constant when the motion vector is in region 3.
0xA7				
	4:0	6h	*kimdet0*	Low-pass constant 0 for input motion detection.
0xA8				
	4:0	4h	*kimdet1*	Low-pass constant 1 for input motion detection.
0xA9				
	4:0	1h	*kimdet2*	Low-pass constant 2 for input motion detection.

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Table 17. Memory Related Control

Sub-Addr	Bits	Default	Name	Description
0x40				
	7	0b	*i2m_siz*	Program enable for the size of the region transferred from the input unit. 0 = region size to be passed directly from the input unit according to Table 7 1 = programming the region size through the *i2m_hlen* and *i2m_vlen* fields.
	6:0	59h	*i2m_hlen*	Width of the region transferred from the input unit. Valid only when *i2m_siz* 0x40[7] = 1. Width = (*i2m_hlen* + 1) x 8 pixels
0x41				
	7:0	77h	*i2m_vlen*	Height of the region transferred from the input unit. The odd field is assumed to include one additional row. Valid only when *i2m_siz* = 1. Height = (*i2m_vlen* + 1) x 2 rows
0x44				
	7	0b	*i2m_offset*	Destination offset enable for data transferred from the input unit. 0 = top left corner to be at coordinate (0,0) 1 = programming the top left corner through the *i2m_left* and *i2m_top.*
	6:0	0h	*i2m_left*	Column coordinate for the top left corner for data transferred from the input unit. Valid only when *i2m_ offset* 0x44[7] = 1. Column coordinate = *i2m_left* x 8
0x45				
	7:0	0h	*i2m_top*	Row coordinate for the top left corner for data transferred from the input unit. Valid only when *i2m_ offset* 0x44[7] = 1. Row coordinate = *i2m_top* x 2

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Table 17. Memory Related Control *(Continued)*

Sub-Addr	Bits	Default	Name	Description
0x46				
	1	0b	*i2m_step*	Step enable for data transferred from the input unit. Valid only when *i2m_freeze* 0x46[0] = 0. *i2m_step* = 0: no skipping. *i2m_step* = 1: skipping enabled. This allows the skipping of *i2m_step_siz* 0x47[7:0] interlaced field pairs between updates from the input unit.
	0	0b	*i2m_freeze*	Freeze enable for data transferred from the input unit. *i2m_freeze* = 0: no freeze. *i2m_freeze* = 1: freeze enabled. This prevents the frame buffer from being updated by the input unit.
0x47				
	7:0	3h	*i2m_step_siz*	Step size for data transferred from the input unit. Specifies the number of field pairs to skip between updates. Valid only when *i2m_step* 0x46[1] = 1 and *i2m_freeze* 0x46[0] = 0.
0x4C				
	2	0b	*bg_status*	Background paint status. High when painting the background. Low otherwise. Read only.
	1	0b	*bg_pattern*	Background pattern control. *bg_pattern* = 0: solid color *bg_pattern* = 1: checkerboard pattern
	0	0b	*bg_ena*	Background paint enable. Background paint is initiated by a rising edge on this bit. *bg_ena* = 0: disabled *bg_ena* = 1: enabled
0x4D				
	7:0	3Ah	*bg_color[7:0]*	Lower order 8 bits of the background color. Used for 'V' data of YUV and 'R' data of RGB fields.
0x4E				
	7:0	48h	*bg_color[15:8]*	Middle order 8 bits of the background color. Used for 'U' data of YUV and 'B' data of RGB fields.
0x4F				
	7:0	70h	*bg_color [23:16]*	Higher order 8 bits of the background color. Used for 'Y' data of YUV and 'G' data of RGB fields.
0x50				
	1:0	2h	*row_len*	Length of a frame buffer row in units of 512 bytes. The default value corresponds to 768 video pixels. Length = *row_len* + 1 units

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Table 17. Memory Related Control *(Continued)*

Sub-Addr	Bits	Default	Name	Description
0x51				
	5	0b	*motion_siz*	Size of a frame buffer motion field in units of 128 kB. The default is configured for NTSC/480i or PAL mode. Valid only when *prim_siz* 0x51[0] = 1.
	4:1	2h	*video_siz*	Size of a frame buffer video field in units of 128 kB. Valid only when *primary_siz* = 1. Corresponds to bits [20:17] of the SDRAM byte address. The default is configured for NTSC/480i or PAL mode. *video_siz* = 0: buffer size = 128 kB *video_siz* = 1: buffer size = 256 kB
	0	0b	*prim_siz*	Program enable for the memory layout of the frame buffer. When '0' the memory layout is in the default NTSC/480i or PAL configuration. Otherwise the *video_siz* 0x51[4:1] and *motion_siz* 0x51[5] fields apply.
0x56				
	7	-	*m2d_vact*	Vertical active period for the display unit. Read only.
	6	-	*I2m_odd*	Polarity of the incoming interlaced field. Read only *I2m_odd* = 0: even *I2m_odd* = 1: odd
	5	-	*I2m_vact*	Vertical active period for the incoming field. Read only.
	4	0b	*film_phase*	Phase used in film mode merging when under external control. Valid only when *film_ctl* 0x56[2]=1.
	3	0b	*film_mode*	Enables film mode merging of fields instead of standard merging of fields when film data is detected under internal control. Active high. Valid only when *film_ctl* 0x56[2]=0. *film_mode* = 0: standard field merging *film_mode* = 1: film mode field merging
	2	0b	*film_ctl*	Film mode control. *film_ctl* = 0: internal control, in which case *film_mode* 0x56[3] applies. *film_ctl* = 1: external control, in which case *film_phase* 0x56[4] applies.
	1:0	0h	*film_sens*	Sensitivity for detecting film materials *film_sens* = 0: least sensitive *film_sens* = 3: most sensitive

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Table 17. Memory Related Control *(Continued)*

Sub-Addr	Bits	Default	Name	Description
0x57				
	5	0h	*mem_enaN*	Memory controller enable. Active low. Toggle high and then low to reinitialize the memory controller, including the external SDRAM, without having to reset the chip.
	4	0h	*ntsc2pal*	Rate conversion enable, especially for NTSC (60 Hz) to PAL (50 Hz), or 480p (60 Hz) to 576p (50 Hz).
	3:2	0h	*latency*	Read latency. Read latency = *latency* + 3 cycels
	1:0	0h	*ref_len*	Refresh length.
0x58				
	7	0b	*m2d_offset*	Source offset enable for data transferred from the frame buffer. 0 = the top left corner be at coordinate (0,0) 1 = programming the top left corner through the *m2d_left* 0x58[6:0] and *m2d_top* 0x59[7:0] fields
	6:0	0h	*m2d_left*	Column coordinate for the top left corner of the frame buffer. Valid only when *m2d_ offset* = 1. Column coordinate = *m2d_left* x 8
0x59				
	7:0	0h	*m2d_top*	Row coordinate for the top left corner of the frame buffer. Valid only when *m2d_ offset* = 1. Row coordinate = *m2d_top* x 2
0x5C				
	7	0b	*m2d_siz*	Program enable for the size of the region transferred from the frame buffer. *m2d_siz* = 0: region size to be passed directly from the input unit according to Table 7 *m2d_siz* = 1: programming the region size through the *m2d_hlen* and *m2d_vlen* fields.
	6:0	59h	*m2d_hlen*	Width of the region transferred from the frame buffer. Valid only when *m2d_siz* 0x5C[7] = 1. Width = (*m2d_hlen* + 1) x 8 pixels
0x5D				
	7:0	77h	*m2d_vlen*	Height of the region transferred from the frame buffer. The odd field is assumed to include one additional row. Valid only when *m2d_siz* = 1. Height = (*m2d_vlen* + 1) x 2 rows

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Table 18. Display Related Control

Sub-Addr	Bits	Default	Name	Description
0x60				
	2	0b	*il_output*	Interlaced output format enable. *il_output* = 0: progressive output. *il_output* = 1: interlaced output.
	1	0b	*dsp_sync*	Program enable for output syncs. *dsp_sync* = 0: the output sync timing is given by Table 10 *dsp_sync* = 1: programmed by fields (0x61..0x6A)
	0	1b	*dsp_ena*	Enable bit for the entire display unit. Display unit operation is started when a rising edge is detected on this bit, stopped on a falling edge.
0x61				
	1	0b	*vsq_polN*	Pin VSq polarity. *vsq_polN* = 0: active high *vsq_polN* = 1: active low
	0	0b	*hsq_polN*	Pin HSq polarity. *hsq_polN* = 0: active high *hsq_polN* = 1: active low
0x62				
	7:0	40h	*hsp*	Horizontal sync pulse length in pixels. Valid only when *dsp_sync* 0x60[1] = 1.
0x63				
	7:0	48h	*hbp*	Horizontal blanking pulse length in pixels. Valid only when *dsp_sync* 0x60[1] = 1.
0x64				
	7:0	5Ah	*hap*	Horizontal active-video pulse length. Valid only when *dsp_sync* 0x60[1] = 1. Horizontal pulse Length = *hap* x 8 pixels
0x65				
	7:0	5Ah	*hlp[7:0]*	Lower 8 bits of horizontal total line length in pixels. Valid only when *dsp_sync* 0x60[1] = 1.
0x66				
	3:0	3h	*hlp[11:8]*	Upper 4 bits of horizontal total line length in pixels. Valid only when *dsp_sync* 0x60[1] = 1.
0x67				
	7:0	2h	*vsp*	Vertical sync pulse length in lines. Valid only when *dsp_sync* 0x60[1] = 1.
0x68				
	7:0	1Ah	*vbp*	Vertical blanking pulse length in lines. Valid only when *dsp_sync* 0x60[1] = 1.

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Table 18. Display Related Control *(Continued)*

Sub-Addr	Bits	Default	Name	Description
0x69				
	7:0	7Ch	*vap*	Vertical active-video pulse length. Valid only when *dsp_sync* 0x60[1] = 1. Vertical pulse length = *vap* x 4 lines.
0x6A				
	7:0	0Dh	*vlp[7:0]*	Lower 8 bits of total vertical length in lines. Valid only when *dsp_sync* 0x60[1] = 1.
0x6B				
	3:0	2h	*vlp[11:8]*	Upper 4 bits of total vertical length in lines. Valid only when *dsp_sync* 0x60[1] = 1.
0x6C				
	7:0	2h	*vbp_e*	Vertical blanking pulse length for even field of interlaced output. In lines. Valid only when *dsp_sync* (0x60:1) = 1.
0x70				
	2	1b	*di_bypass*	Deinterlace bypass. *di_bypass* = 0: no bypass *di_bypass* = 1: interlaced data is de-interlaced *without* undergoing vertical or angle interpolation or motion compensation.
	1	0b	*vert_interp*	Vertical linear interpolation enable. *vert_interp* = 0: angle interpolation *vert_interp* = 1: vertical linear interpolation
	0	1b	*dsp_422_conv*	Method for converting from 4:1:1 to 4:2:2 or from 4:2:2 to 4:4:4 formats in the *display unit*. *dsp_422_conv* = 0: copy the UV sample *dsp_422_conv* = 1: bilinear interpolation.
0x71				
	4	0b	*us_siz*	Program enable for output scaling region size. *us_siz* = 0: scaling region size disabled *us_siz* = 1: the size is given by the *us_hlen* 0x73[7:0] and *us_vlen* 0x72[7:0] fields, regardless of the value of the *us_remap* 0x71[0] field.
	3:1	0h	*us_mode*	Programmable output resolution mode defined by Table 11. Valid only when *us_remap* is set to 1.
	0	0b	*us_remap*	Program enable for the output resolution mode. *us_remap* = 0: the output resolution is same as the input resolution. *us_remap* = 1: remapping of the output mode through the *us_mode* (0x71:3-1) field.

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Table 18. Display Related Control *(Continued)*

Sub-Addr	Bits	Default	Name	Description
0x72				
	7:0	59h	*us_hlen*	Width of the output display device. Width = (*us_hlen* + 1) x 8 pixels
0x73				
	7:0	77h	*us_vlen*	Height of the output display device. Valid only when *us_siz* 0x71[4] = 1. Height = (*us_vlen* + 1) x 4 rows
0x78				
	7	1b	*blue_screen*	Blue screen enable. Active high.
	6	0b	*y_blank*	Blanking value for Y when fixing the blanking values for YUV. *y_blank* = 0: blanking value = 64 *y_blank* = 1: blanking value = 0
	5	0b	*color_lut*	Color LUT enable. Active high.
	4:3	0h	*prim_cs*	Input color space. Refer to Table 12.
	2:0	0h	*common_cs*	Common output color space. Refer to Table 13.
0x79				
	7:0	10h	*y_blue*	Blue screen value of Y (G) component. Valid only when *blue_screen* (0x78:6) = 1.
0x7A				
	7:0	80h	*u_blue*	Blue screen value of U (B) component. Valid only when *blue_screen* (0x78:6) = 1.
0x7B				
	7:0	80h	*v_blue*	Blue screen value of V (R) component. Valid only when *blue_screen* (0x78:6) = 1.
0x98				
	1	1b	*load_status*	Load status. High when loading the internal LUT's from the ROM. Low otherwise. Read only.
	0	0b	*lut_load*	Load enable for internal LUT's from ROM. The load sequence is initiated by a rising edge on this bit.
0x99				Individual internal LUT load activation. When any bit is '1', the corresponding LUT is loaded from ROM on a rising edge of *lut_load* (0x98:0).
	4	0b	*color_lut_load*	Color LUT load enable.
	3	0b	*hue_load*	Hue LUT load enable.
	2	0b	*hscaler_load*	Horizontal up scaler LUT enable.
	1	0b	*vscaler_load*	Vertical up scaler LUT enable.
	0	0b	-	Reserved.

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Table 18. Display Related Control *(Continued)*

Sub-Addr	Bits	Default	Name	Description
0x9C				
	7:0	0h	*lut_addr[7:0]*	Lower 8 bits of the LUT address.
0x9D				
	3:0	0h	*lut_addr[11:8]*	Upper 4 MSB of the LUT address.
0x9E				
	7:0	0h	*lut_dat*	Data to or from the internal LUT's. When written, writes the value *lut_dat* to the location *dsp_lut_addr* ({0x9D:3-0, 0x9C}). When read, returns the value stored at the same location.
0xD0				
	4:0	2h	*khpw*	High-pass peaking filter weighting.
0xD1				
	4:0	2h	*kbpw*	Band-pass peaking filter weighting.
0xD2				
	2:0	1h	*klp*	Low-pass peaking filter gain.
0xD3				
	5:0	8h	*peak_coring*	Coring threshold for peaking. *peak_coring* = 0: peaking is off Coring threshold = *peak_coring*
0xD4				
	7:3	8h	*dlti_coring*	Coring threshold for DLTI. *dlti_coring* = 0: DLTI is off Coring threshold = *dlti_coring* x 2
	2:0	0h	*dlti_gain*	Gain for DLTI. DLTI is disabled when *dlti_gain* = 0.
0xD5				
	7:4	8h	*dcti_coring*	Coring threshold for DCTI. *dcti_coring* = 0: DCTI is off Coring threshold = *dcti_coring* x 2
	3	0b	*dcti_slow*	Bandwidth mode of DCTI. *dcti_slow* = 0: high-bandwidth *dcti_slow* = 1: low-bandwidth
	2:0	0h	*dcti_gain*	Gain for DCTI. DCTI is disabled when *dcti_gain* = 0.
0xD6				
	5:0	20h	*contrast*	Contrast adjustment. Contrast adjustment is disabled when *contrast* = 32.

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Table 18. Display Related Control *(Continued)*

Sub-Addr	Bits	Default	Name	Description
0xD7				
	7:0	0h	*brightness*	Brightness adjustment, in signed notation. Note that '7f' corresponds to +127, '80' to –128, '81' to –127, etc. Brightness adjustment is disabled when *brightness* = 0.
0xD8				
	7:0	0h	*hue*	Hue adjustment. Hue adjustment is disabled when *hue* is set to 0.
0xD9				
	7:0	40h	*saturation*	Saturation adjustment. Saturation adjustment is disabled when *saturation* = 64.
0xDA				
	7:0	0h	*hue_sin[7:0]*	Lower 8 bits of sin θ as used in the hue calculation, where sin θ is a signed integer –256 .. 256. Read only.
0xDB				
	1:0	0h	*hue_sin[9:8]*	Upper 2 bits of sin θ. Read only.
0xDC				
	7:0	0h	*hue_cos[7:0]*	Lower 8 bits of cos θ as used in the hue calculation, where cos θ is a signed integer –256 .. 256. Read only.
0xDD				
	1:0	0h	*hue_cos[9:8]*	Upper 2 bits of cos θ. Read only.
0xDE				
	4:0	0h	*ble_gain*	Gain for black level expansion. Black level expansion is disabled when *ble_gain* or *ble_thr* is set to 0.
0xDF				
	7:0	0h	*ble_thr*	Threshold for black level expansion. Maximum Y value for consideration for black level expansion.

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Table 18. Display Related Control *(Continued)*

Sub-Addr	Bits	Default	Name	Description
0xE0				
	2	0b	*cgms_prog*	Must be set to 0.
	1	0b	*cgms_standard*	CGMS Standard. Enter '0' for EIA-805 or '1' for EIAJ-CPR 1204.
	0	0b	*cgms_ena*	CGMS Enable.
0xE7				
	7:0	0h	*cgms_dat1*	CGMS Data byte 1.
0xE8				
	7:0	0h	*cgms_dat2*	CGMS Data byte 2.
0xE9				
	7:0	0h	*cgms_dat3*	CGMS Data byte 3.
0xEA				
	1	0b	*p525_ena*	Macrovision copy protection enable. When '1', enables sync embedding and optional CGMS and Macrovision copy protection. When '0', bypasses copy protection processing.
	0	0b	*macro_ena*	Macrovision enable.
0xEA				
	1	0b	*p525_ena*	Macrovision copy protection enable. When '1', enables sync embedding and optional CGMS and Macrovision copy protection. When '0', bypasses copy protection processing.
	0	0b	*macro_ena*	Macrovision enable.

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Table 19. System Related Control

Sub-Addr	Bits	Default	Name	Description
0x10				
	4	0b	*mclk_bypass*	Bypass enable for *mclk* PLL. *mclk_bypass* = 1: *mclk* = *fclk*.
	3:2	0h	*dclk_source*	Source of display clock. ***dclk_source*** / **Description** 00 — *dclk* PLL. PLL is driven by the crystal oscillator input. 01 — dvd_clk. Video input clock. 10 — ext_dclk. External display clock. 11 — Reserved.
	1	1b	*dclk_ena*	Reprogram enable for *dclk* PLL. The *dclk* PLL is reprogrammed using *dclk_freq* (0x12) on a rising edge of this bit.
	0	1b	*mclk_ena*	Reprogram enable for *mclk* PLL. The *mclk* PLL is reprogrammed using *mclk_freq* 0x11on a rising edge of this bit.
0x11				
	7:0	50h	*mclk_freq*	Memory clock frequency in MHz. Clamped at a minimum of 0x10 (16 MHz) and a maximum of 0xC0 (192 MHz). Assumes a 10 MHz source for the *mclk* PLL.
0x12				
	7:0	36h	*dclk_freq*	Twice the display clock frequency in MHz. Clamped at a minimum of 0x10 (16 MHz) and a maximum of 0xC0 (192 MHz). Assumes a 10 MHz source for the *dclk* PLL.
0x14				
	0	0b	*buf_I2c*	I^2C Buffer bit. *buf_I2c* = 0: allow the data of all previous and subsequent I^2C writes to be passed through to the rest of the NV221. *buf_I2c* = 1: buffer subsequent I^2C writes.
0x90				
	7:4	6h	*slave_address [5:2]*	Base device address. Always fixed 6.
	3:2	0h	*slave_address [1:0]*	Configurable lower 2 bits of the base device address. Bit 3 is determined by pin *I2c_a2* and bit 2 by *I2c_a1*. Read only.
	1	0b	*word_address[8]*	Upper bit of word address of the next byte access. In conjunction with the lower 8 bits 0x91[7:0], automatically increments after each access. Read only.
	0	1b	*rwN*	I^2C R/W bit. Writing to it has no effect. Always returns '1' on a read.

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Table 19. System Related Control *(Continued)*

Sub-Addr	Bits	Default	Name	Description
0x91				
	7:0	0h	*word_address [7:0]*	Lower 8 bits of word address of the next byte access. In conjunction with the upper 3 bits 0x90[3:1], automatically increments after each access. Read only.
0x92				
	7:0	24h	*bta[7:0]*	Lower 8 bits of bus turn around time. Reset value is correct for 100 kb/s I^2C operation. *bta* = 0: 1 cycle *bta* = 1: 2 cycles
0x93				
	1	1b	*i2c_filter*	Enables one-clock buffering of incoming I^2C signals to filter out noise.
	0	0b	*bta[8]*	Upper bit of bus turn around time.
0x94				
	7:0	0h	*ram_addr[7:0]*	Least significant 8 bits of the SDRAM address.
0x95				
	7:0	0h	*ram_addr[15:8]*	Second-order 8 bits of the SDRAM address.
0x96				
	6:0	0h	*ram_addr[22:16]*	Most significant 7 bits of the SDRAM address.
0x97				
	7:0	0h	*ram_dat*	Data to or from the SDRAM. When written, writes the value *ram_dat* to the location *ram_addr* (0x94 – 0x96). When read, returns the value stored at the same location. The value of *ram_addr* is incremented at the conclusion of a write or read at this address.

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Table 20. I²C-Bus operation

Sub-Addr	MSB 7	6	5	4	3	2	1	LSB 0
10				***mclk_ bypass***	***dclk_source***		***dclk_ena***	***mclk_ena***
				0	0		1	1
11	***mclk_freq***							
	50							
12	***dclk_freq***							
	36							
14								***buf_I2c***
	-							0
28			***video_err***	***input_format***			***input_type***	
	-		0	0			0	
29			***dvd_mode***		***uv_encode***		***clk_del***	***clk_edge***
	-		2		2		0	0
2A		***hsdvd_pol***	***vsdvd_pol***	***422_conv***	***detect_ form***			***offset***
	-	0	0	1	1	0	0	0
2B	***hsta[7:0]***							
	7A							
2C	***odd_vsta***							***hsta[8]***
	10							0
2D		***even_vsta***						
	-	10						
30							***il_srstN_fb***	***srstN***
	-						1	1
33						***mn_testN***	***mn_ chroma***	***mn_ bypass***
	-					1	1	0
40	***I2m_siz***	***I2m_hlen***						
	0	59						
41	***I2m_vlen***							
	77							
44	***I2m_offset***	***i2m_left***						
	0	0						

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Table 20. I²C-Bus operation (Continued)

Sub-Addr	MSB 7	6	5	4	3	2	1	LSB 0
45	***i2m_top***							
	0							
46							***i2m_step***	***i2m_freeze***
	-						0	0
47	***i2m_step_siz***							
	3							
4C						***bg_status***	***bg_pattern***	***bg_ena***
	-					0	0	0
4D	***bg_color[7:0]***							
	3A							
4E	***bg_color[15:8]***							
	48							
4F	***bg_color[23:16]***							
	70							
50							***row_len***	
	-						2	
51			***motion_siz***	***video_siz***				***prim_siz***
	-		0	2				0
56	***m2d_vact***	***l2m_odd***	***l2m_vact***	***film_phase***	***film_mode***	***film_ctl***	***film_sens***	
			0	0	0	0	0	
57			***mem_enaN***	***ntsc2pal***	***latency***		***ref_len***	
	-		0	0	0		0	
58	***m2d_offset***	***m2d_left***						
	0	0						
59	***m2d_top***							
	0							
5C	***m2d_size***	***m2d_hlen***						
	0	59						
5D	***m2d_vlen***							
	77							

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Table 20. I²C-Bus operation (Continued)

Sub-Addr	MSB 7	6	5	4	3	2	1	LSB 0
60						***il_output***	***dsp_sync***	***dsp_ena***
	-					0	0	1
61							***vsq_polN***	***hsq_polN***
	-						0	0
63	***hsp***							
	40							
63	***hbp***							
	48							
64	***hap***							
	5A							
65	***hlp[7:0]***							
	5A							
66					***hlp[11:8]***			
	-				3			
67	***vsp***							
	2							
68	***vbp***							
	1A							
69	***vap***							
	7C							
6A	***vlp[7:0]***							
	0D							
6B					***vlp[11:8]***			
	-				2			
6C	***vbp_e***							
	2							
70						***di_bypass***	***vert_interp***	***dsp_422_conv***
	-					1	0	1
71				***us_siz***	***us_mode***			***us_remap***
	-			0	0			0

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Table 20. I²C-Bus operation (Continued)

Sub-Addr	MSB 7	6	5	4	3	2	1	LSB 0
72	***us_hlen***							
	59							
73	***us_vlen***							
	77							
78	***blue_ screen***	***y_blank***	***color_lut***	***prim_cs***		***common_cs***		
	1	0	0	0		0		
79	***y_blue***							
	10							
7A	***u_blue***							
	80							
7B	***v_blue***							
	80							
90	***slave_address [5:2]***				***slave_address [1:0]***		***word_ address[8]***	***rwN***
	6				0		0	1
91	***word_address [7:0]***							
	0							
92	***bta [7:0]***							
	24							
93	-	-	-	-	-	-	***i2c_filter***	***bta [8]***
							1	0
94	***ram_addr [7:0]***							
	0							
95	***ram_addr [15:8]***							
	0							
93	-	***ram_addr [22:16]***						
		0						
97	***ram_dat***							
	0							
98							***load_ status***	***lut_load***
	-						1	0

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Table 20. I²C-Bus operation (Continued)

Sub-Addr	MSB 7	6	5	4	3	2	1	LSB 0
99				***color_lut_load***	***hue_load***	***hscaler_load***	***vscaler_load***	**-**
	-			0	0	0	0	0
9C	***lut_addr[7:0]***							
	0							
9D					***lut_addr [11:8]***			
	-				0			
9E	***lut_dat***							
	0							
A0	***im_thr0***							
	3							
A1	***im_thr1***							
	6							
A2	***im_thr2***							
	A							
A3	***knrf0***							
	40							
A4	***knrf1***							
	54							
A5	***knrf2***							
	68							
A6	***knrf3***							
	80							
A7				***kimdet0***				
	-			6				
A8				***kimdet1***				
	-			4				
A9				***kimdet2***				
	-			1				
D0				***khpw***				
	-			2				

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Table 20. I²C-Bus operation (Continued)

Sub-Addr	MSB 7	6	5	4	3	2	1	LSB 0
D1				***kbpw***				
	-			2				
D2						***klp***		
	-					1		
D3			***peak_coring***					
	-		8					
D4	***dlti_coring***					***dlti_gain***		
	8					0		
D5	***dcti_coring***				***dcti_slow***	***dcti_gain***		
	8				0	0		
D6			***contrast***					
	-		20					
D7	***brightness***							
	0							
D8	***hue***							
	0							
D9	***saturation***							
	40							
DA	***hue_sin[7:0]***							
	0							
DB							***hue_sin[9:8]***	
	-						0	
DC	***hue_cos[7:0]***							
	0							
DD							***hue_cos[9:8]***	
	-						0	
DE					***ble_gain***			
	-				0			
DF	***ble_thr***							
	0							

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Table 20. I²C-Bus operation (Continued)

Sub-Addr	MSB 7	6	5	4	3	2	1	LSB 0
E0						***cgms_prog***	***cgms_ standard***	***cgms_ena***
	-					0	0	0
E7	***cgms_dat1***							
	0							
E8	***cgms_dat2***							
	0							
E9	***cgms_dat3***							
	0							
EA							***p525_ena***	***macro_ena***
	-						0	0

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8 LIMITING VALUES

Table 21. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage	VDD	-0.5 to 5.0	V
Voltage on any pin	Vpin	-0.5 to 5.0	V
Ambient (Case) temperature	Ta	-10 to 70	°C
Storage temperature	Ts	-65 to 150	°C

9 CHARACTERISTICS

Table 22. D/A converters DC characteristics
(qvrefin=1.313V; RL=37.5ohm, CL=15pF; qres=100ohm; Temp=75^{o}C, unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating voltage range	qdvdd qavdd yqavdd uqavdd bqavdd	3.0	3.3	3.6	V	
yqavdd supply current	IAVDDG	--	38.34	--	mA	SL=0, SLG=0
uqavdd supply current	IAVDDB	--	38.34	--	mA	SL=0, SLB=0
vqavdd supply current	IAVDDR	--	38.34	--	mA	SL=0, SLR=0
qavdd supply current	IAVDD	--	2.75	--	mA	SL=0
qdvdd supply current	IVDD	--	TBD	--	mA	fully active @100MHz.
Full scale current	IOFS	2.00	34.08	--	mA	.
Output voltage range	V(IO)	--	1.28	--	V	
DAC resolution	--	--	10	--	bits	
Integral non-linearity error	INL	--	-0.5	+-2	LSB	
Differential non-linearity error	DNL	--	+-0.5	+-1	LSB	

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Table 23. D/A converters AC characteristics
(qdvdd=qavdd=3.3V; yqavdd=uqavdd=vqavdd=3.3V; qvrefin=1.313V; RL=37.5ohm, CL=15pF; qres=100ohm; Temp=75^{o}C, unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
dclk period	Tck	5.64	--	--	ns	
dclk to valid output	Tdelay	--	2.93	4.53	ns	
Output rise time	Tr	--	1.69	2.57	ns	10% to 90% IOFS.
Output fall time	Tf	--	1.75	2.79	ns	90% to 10% IOFS.
Output settling time	Tsettle	--	5.64	8.82	ns	
Glitch energy	--	--	4.86	--	pvs	
DAC to DAC crosstalk	--	--	TBD	--	dB	

Table 24. Core and I/O DC characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Power supply to all power pins	VDD	3.0	3.3	3.6	V	
Total power supply current	IDD			300	MA	
High level input voltage	Vih	2.0	.7VDD		V	
Low level input voltage	Vil		.3VDD	0.8	V	
High level output voltage	Voh	2.4			V	Ioh = -4.0ma
Low level output voltage	Vol			0.4	V	Iol = 4.0ma

Table 25. Input/Output Timing

Parameter	Symbol	Min	Type	Max	Unit	Condition
Input data (din) setup time	t_{su}	-	-	5	ns	
Input data (din) hold time	t_h	-	-	6	ns	
dclk, clock cycle time					ns	
dclk, clock duty cycle		40	-	60	%	
dclk, clock rise time				-	ns	
dclk, clock fall time				-	ns	

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10 APPLICATION INFORMATION

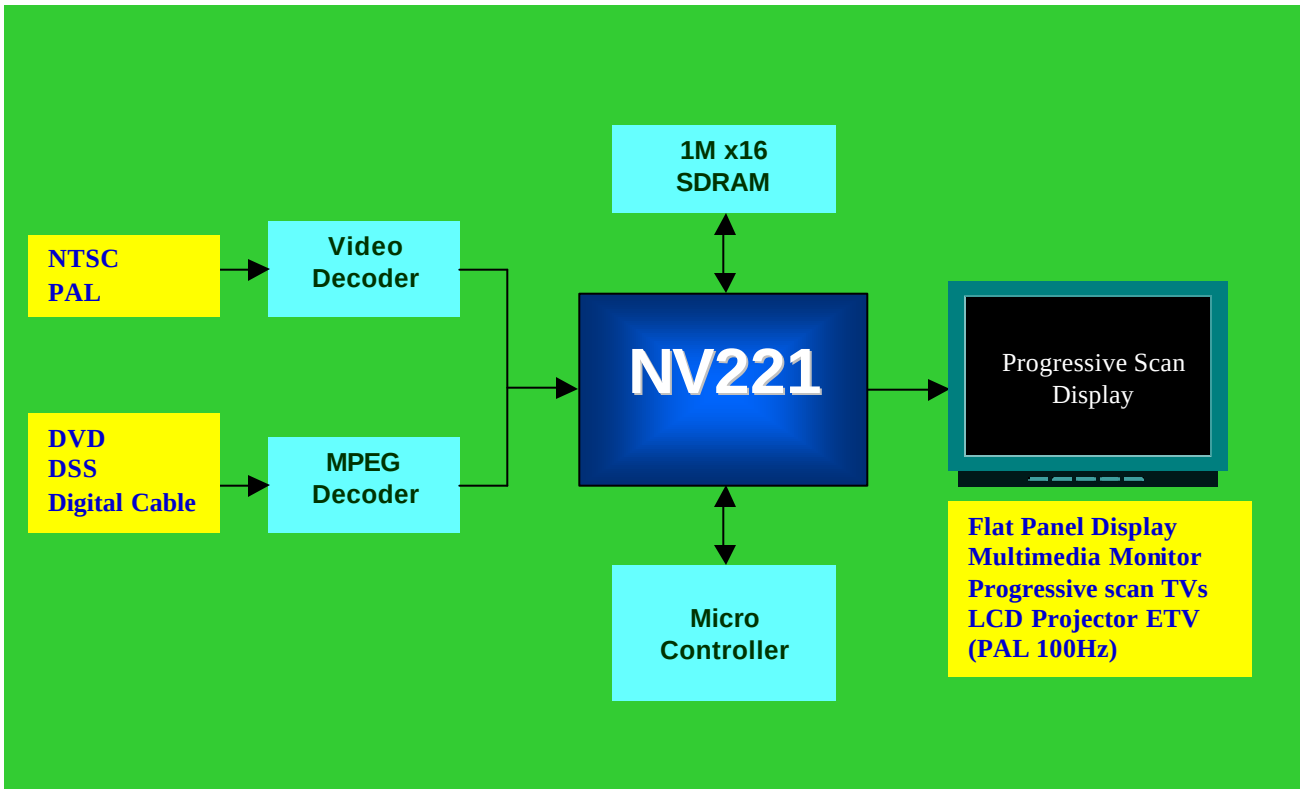


Figure 10. Video Display Processor Block Diagram

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11 PACKAGE DIMENSIONS

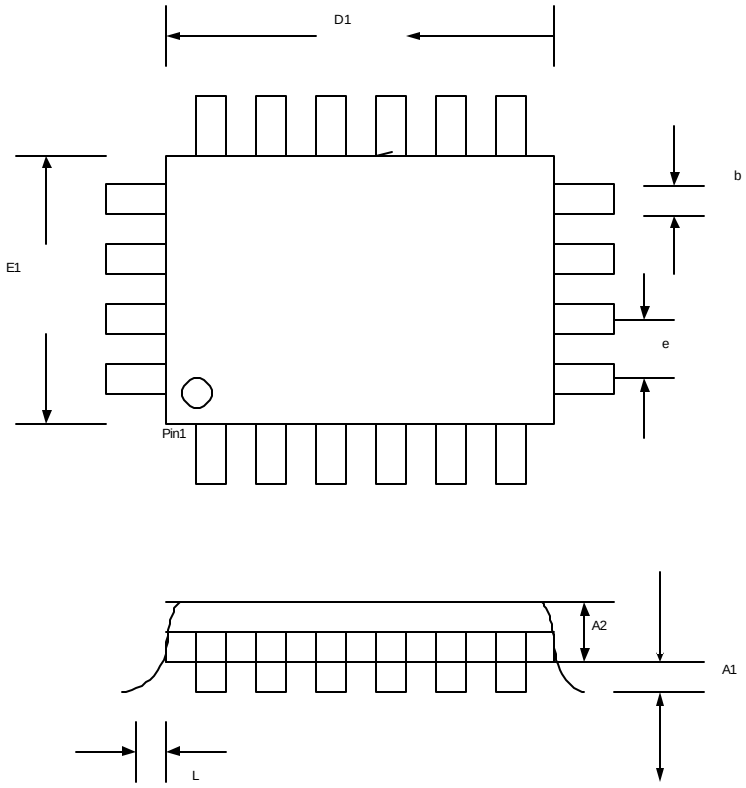
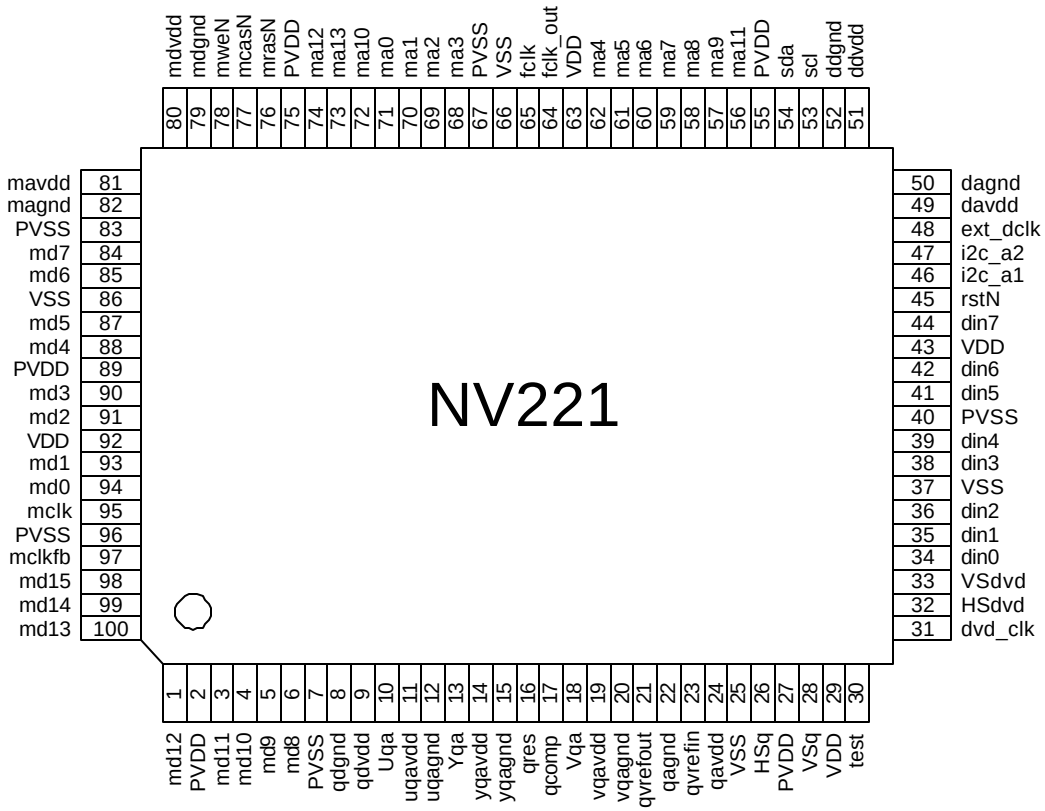


Table 26. Package Dimensions for 100-pin PQFP

	Description	Dimensions (mm)
D1	Width	20
E1	Height	14
A1	Stand-off	0.25
A2	Body thickness	2.72
L1	Lead length	1.6/1.8/1.95
b	Lead width	0.3
c	Lead thickness	0.15
e	Lead pitch	0.65

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12 PIN CONNECTION DIAGRAM



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