eCOG1X Microcontroller Product Family

The **eCOG1X** microcontroller family is a range of low-power microcontrollers, based on a 16-bit Harvard architecture with a 24-bit linear code address space (32Mbyte) and 16-bit linear data address space (128Kbytes). The devices are highly configurable, with options including combinations of USB 2.0 OTG, 10/100 Ethernet MAC and analogue I/O. Each combination is available with different onboard memory options, with up to 512Kbytes of FLASH and 24Kbytes of SRAM. Products are available in a variety of QFN and BGA packages with pin counts between 68 and 208 pins. Comprehensive Development and Evaluation Kits are available. All are fully supported by Cyan's free, class-leading, integrated development environment, **CyanIDE**, which includes automatic peripheral configuration and an unrestricted ANSI C Compiler.

- 0 to 70MHz 1.8V core
- 3.3V I/O (some pins 5V tolerant)
- Powerful arithmetic operations
- Barrel Shifter
- Harvard Architecture
- Built in Emulator (eICE)
- Low power operation
- 512/384/256/128Kbytes FLASH
- 24Kbytes SRAM
- MMU
- Power-saving code cache
- Code security feature
- External Host Interface
- External Memory Interface
- Fast Vectored Interrupts
- 2 off DUARTs
- DUSART/ SPI/ I^2C / SCI/ IR
- SPI
- I^2S
- Separate Dual SCI
- Dual 7 channel 12-bit ADCs
- Dual 12-bit DACs
- Temperature Sensor
- Supply Voltage Sensor
- Power-On Reset
- USB 2.0 OTG 480Mbit/s
- 10/100 Ethernet MAC
- 4x32 LCD Controller
- 5 Multi Purpose Timers
- - Clock timer
- - 2 off counter / timer
- - 2 off PWM timer
- Watchdog Timer
- Long Interval Timer
- PWM motor control timers
- Parallel Interface
- 116 General Purpose I/O pins
- Low power relaxation oscillator
- Interfaces to 8/16/32-bit parts

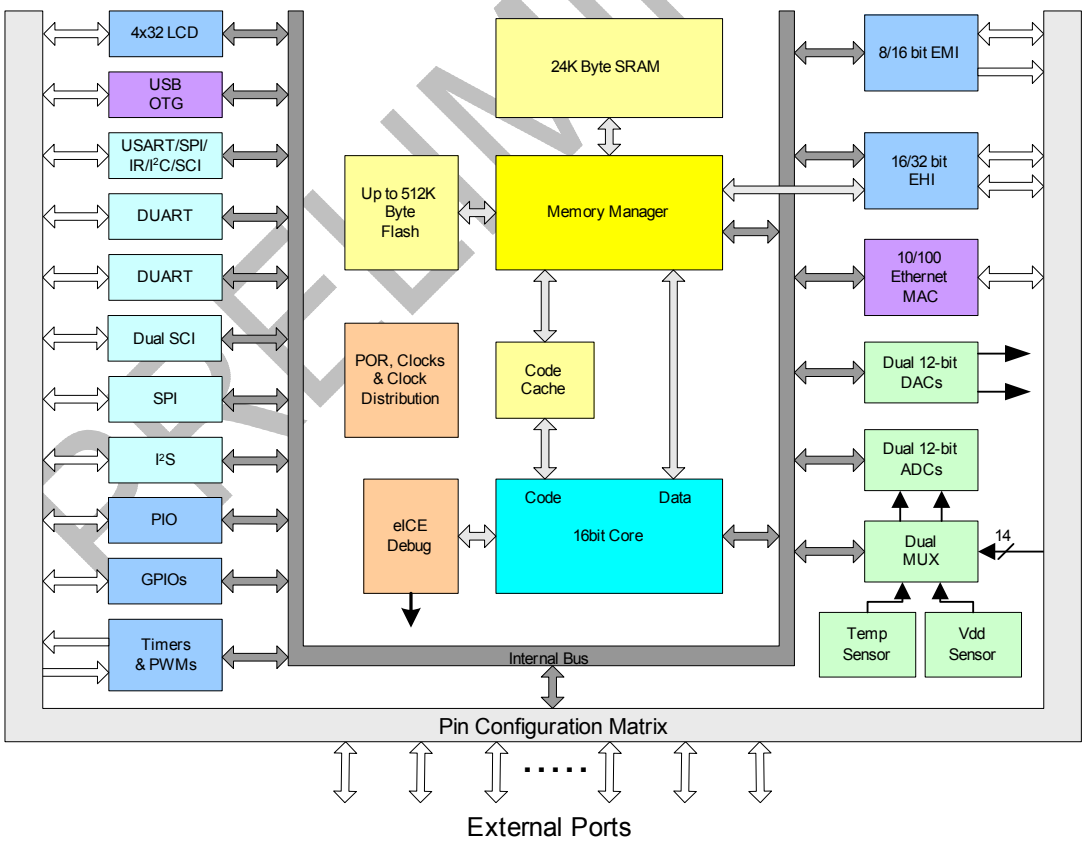


Figure 1 Internal Block Diagram

CPU Core
- 16-bit 70MHz core.
- Harvard architecture.
- Supports a full array of 16-bit arithmetic operations, including both signed and unsigned MULtiply and DIVide instructions.
- 32Mbyte code address space.
- 128Kbyte data address space.
- Vectored interrupts.
- Full ICE debug support.

MMU
- Performs logical to physical address translations.
- Translates between RAM, Program Memory, and external memory devices for both code and data accesses concurrently.
- Lookup tables in RAM or Flash can be mapped between each memory area.
- Up to four concurrent translations to external devices from code addresses.
- Up to four concurrent translations to external devices from data addresses.
- Programmable wait state generation.
- Concurrent accesses to same device are prioritised.
- Translations are prioritised to allow overlapped translations.

Flash Memory
- 512/256/128Kbytes.
- Organised into multiple sectors.
- Can be mapped into both code and data spaces.
- Individual Flash sectors can be read and/or write protected.
- Simple programming via JTAG interface, with eICE support for programming for user access.

Code Cache
- Individual cache entries can be locked.
- Can cache both User and Interrupt Mode.

Static RAM
- 24Kbytes.
- Can be mapped into both code and data spaces.

External Memory Interface (EMI)
- 8 or 16-bit data bus.
- 16 or 24-bit address bus.
- Multiplexed address/data for 16-bit data bus.
- External devices can be mapped into both code and data space.
- Supports SRAM (bus) and SDRAM interface modes.
- Supports up to 256Mb Single Data Rate 16-bit wide SDRAMs.
- Four Row/Column SDRAM address multiplexing schemes.
- Supports SDRAM auto and self refresh.
- Configurable timing.
- Supports low power SDRAM suspend/standby mode.
- Single cycle data space access, code space burst access in conjunction with Code Cache.
- Hardware support for software initialisation and refresh of SDRAM.

External Host Interface (EHI)
- Provides an interface to an external host processor or FIFO.
- Supports both DMA and memory mapped peripheral modes.
- Interrupt generated upon transfer.

DMA Mode:
- Supports master and slave mode timings.
- 16/32-bit data bus.
- Request & Acknowledge control lines.
- Configurable master mode timing.
- DMA connection into internal SRAM (11-bit block address, max 256 byte block size).
- Internal DMA controller supports circular and linked list buffer models.

Memory Mapped Mode:
- Selectable block size
  256 x 16-bit data
  8 x 32-bit data.
- Three control lines: chip select, read/write direction and wait.
- Configurable control line senses.

DUARTs

- Two independent dual UART modules.
- Each DUART has two asynchronous double-buffered RS232-compatible serial ports.
- Supports 5, 6, 7, or 8 data bits.
- 1, 1.5 or 2 stop bits.
- Even, odd or no parity.
- Automatic end-of-frame guard time insertion of 0 to 64 bit periods.
- Receive timeout detection 0 to 64 bit periods.
- Software Line Break generation.
- Programmable Baud rate generator.
- Interrupts generated on full and empty.
- Receiver error detection for false start bits, parity errors and frame errors.
- Configurable data polarity.
- Oversampling of received data for noise immunity.

DUSART

- Two synchronous/asynchronous double-buffered serial ports.
- Programmable Baud rate generator.
- End of frame guard time insertion of 0 to 64 bit periods.
- Receive timeout detection 0 to 64 bit periods.
- Receiver error detection for false Start bits, Parity errors, Frame errors and Buffer overflow.
- Configurable data and clock polarity.
- Configurable data packing, MSB or LSB first.
- Oversampling of receive data for noise immunity.

Asynchronous Interface:

- Asynchronous frame support for 5, 6, 7 or 8 bits of data.
- 1, 1.5 or 2 stop bits.
- Even, odd or no parity.
- Full modem support using GPIO.
- Software Line Break generation.

Synchronous Interface:

- Internal or external transmit and receive clock.
- Full or half duplex.
- Frame sizes from 1 to 16 bits with larger frames possible.
- Support for NRZ, RZ.
- Support for PM, PWM and ASK modulation in conjunction with PWM timer.

I^2C:

- Two wire I^2C compatible port.
- Address matching.
- ACK bit and wait state insertion.
- Multi-master arbitration.
- Supports 10-bit addressing and fast mode.

SPI:

- Multi-slave SPI system.
- Four slave select lines.
- Both master and slave roles.
- Programmable serial clock polarity and phase.
- Support for high speed directly clocked operation and sampled filtered operation.

Smart Card Interface Controller:

- ISO 7816 compatible smart card interface controller.
- Multiprocessor support.
- Byte level support for T=0 protocol.
- Detection and generation of the transmission error signal for T=0 protocol.
- Automatic retransmission of corrupted bytes for T=0 protocol.
- Automatic control of card power switching.
- Hardware state machine for power up, reset and shutdown sequences.
- Clock generation using PWM1 timer.

Infra-Red Link:

- Programmable baud rates.
- Support for low rate (<115.2 kbps) IrDA framing and modulation.
- Compatible with common ASK, PM, PPM (e.g. RC-5) modulation schemes.
- Variable frame lengths up to 255 bits.
- Variable length multi-byte frames.
- Half duplex operation using an integral frame duration (maximum 1023 symbols) to separate transmit and receive exchanges.
- Raw IR mode supported (software modem).
- Programmable start, stop, data length, frame length and polarities.
- Programmable start and stop sequences.
- Support for current and future frame formats.
- Carrier frequency generation using PWM2 timer.

User Serial Port (USR):
- Provides direct access to internal registers of each USART.
- Custom serial protocols may be emulated.
- Up to 255 symbols per frame.
- Parity may be automatically inserted or tested at the end of each frame.
- Start bit edge detection.
- Tx/Rx interrupts.

Dual Smart Card Controller
- Two independent smart card interface controllers.
- ISO 7816 compatible and meets the requirements of the EMV 2000 specification.
- Multiprocessor support.
- Byte level support for T=0 protocol.
- Detection and generation of the transmission error signal for T=0 protocol.
- Automatic retransmission of corrupted bytes for T=0 protocol.
- Automatic control of card power switching.
- Hardware state machine for power up, reset and shutdown sequences.
- Flexible clock and Baud rate generation, software selectable.
- Serial ports double buffered for both transmit and receive data.

General Purpose I/O (GPIO)
- Up to 116 GPIO pins.
- Individually configurable as inputs, outputs, or bidirectional.
- Outputs driven, open drain, or tri-state
- Direct drive LEDs.
- Each input can generate an interrupt.

External Interrupts
- Any GPIO can generate an interrupt.
- Level or edge sensitive interrupts.

Parallel Interface (PIO)
- Two 16-bit parallel data ports, configurable as inputs or outputs.
- Outputs driven, open drain, or tri-state.

Timers
- Two 16-bit general purpose timers/event counters.
- Two 16-bit PWM timers.
- 16-bit event capture timer.
- 16-bit clock timer.
- 16-bit watchdog timer.
- 24-bit long interval timer.
- Most timers have prescalers.

Motor Control PWM Timers
- Six PWM outputs specifically targeted for simple motor control.
- Two independent period timers.
- Edge or centre aligned modes of operation.
- Versatile clocking and timing of independent channels.
- Channels can be paired with programmable guard times for high and low side switching.
- Fine control of PWM toggle points for accurate control.

LCD Controller
- Support for direct and multiplexed drive, 1 to 4 common backplane lines.
- Up to 32 data segment lines giving control of up to 128 individual segments.
- Simple register interface.

USB On-The-Go
- Complies with USB standard for high-speed functions and *On-The-Go* supplement to USB 2.0 specification.
- USB *On-The-Go* (OTG) Dual Role device, supports point-to-point communications with one high-speed, full-speed or low-speed device.
- Full USB 2.0 OTG support via external ULPI interface, allowing high speed 480 Mbit/s transfer rate.
- Supports Session Request and Host Negotiation protocol.
- Supports Suspend and Resume signalling.
- Supports a low-speed, full-speed or high-speed single device when operating as a host.
- Supports full-speed or high-speed data transfer as a peripheral.
- Full and low speed operation support through an on-chip serial PHY.
- Fast, efficient DMA to internal memory for endpoint data.
- Uses 4Kbytes of internal SRAM as a dedicated endpoint data buffer.

10/100 Ethernet MAC
- Supports 10/100 Mb/s data transfer rate.
- Meets IEEE 802.3 CSMA/CD standard
- Full or half duplex operation.
- Dedicated separate 64 byte receive and transmit buffers.
- Hardware address filtering.
- Power saving features including suspend and stop.
- Fast, efficient DMA to internal memory, supporting chained or ring based buffer descriptors.

I^2S
- Inter-IC Sound standard (I2S) compatible serial interface.
- One receive channel and one transmit channel.

ESPI
- Enhanced SPI peripheral, separate from the DUSART.
- Data transfer size of 8 to 16 bits.
- Four slave select lines.
- Operates as master or slave device.
- Programmable serial clock polarity and phase.
- Support for multiple transfers with programmable delay times.

Dual 12-bit ADCs
- Dual 12-bit successive approximation ADCs, with 10 bit, 8 bit and 6 bit modes for faster conversion.
- Dual sample/holds for simultaneous sampling of two channels.
- Up to 800 ks/s 6 bit on each ADC.
- Up to 500 ks/s 8 bit on each ADC.
- Up to 350 ks/s 10 bit on each ADC.
- Up to 200 ks/s 12 bit on each ADC.
- Dual 7 channel analogue input multiplexers with automatic sequencing. (Fewer channels available in the smaller packages)
- Single ended or differential conversion modes.
- Conversion trigger from internal or external timer event.
- Extended sample period for high impedance sources.
- On-chip temperature sensor.
- On-chip power supply monitor.

Dual 12-bit DACs
- Maximum conversion time 4us (settling to ±1 LSB).
- 12 bits resolution.
- Asynchronous (software triggered) or synchronous (timer triggered) conversion modes.
- Two channel synchronous mode.
- DAC ready interrupt and wakeup facility.

Clocks
- Uses one or two quartz crystals, a low cost 32 kHz watch crystal and/or a higher frequency 5 to 10 MHz crystal for reduced clock jitter (8 MHz nominal).
- Two independent programmable PLLs enabling a wide range of synthesised clock frequencies.
- Can generate internal clock frequencies up to 200 MHz.
- Low power relaxation oscillator, with or without external tuning resistor, 1 MHz to 11 MHz operation providing instant clock startup.
- Selection of clock source and PLL frequency under software control.

C Compiler suite
- ANSI C Compiler.
- Validated to ANSI/ISO/FIPS-160.
- ANSI Standard Library.
- Macro Assembler.
- Software Simulator and debugger.

eICE Debugger Interface
- Real-time debug port.
- eICE can program internal Flash.
- When BREAK command is locked in the cache, provides a large number of address breakpoints.
- Commands include Reset, Stop, Run, Run to Break.
- Non-intrusive read and write to any core register, including PC.
- Read and write of any memory location.

JTAG
- Access for test and boundary scan.
- Fast flash programming.

Power Saving Features
- Sleep mode with wake on interrupts.
- All peripherals can be stopped when not in use.

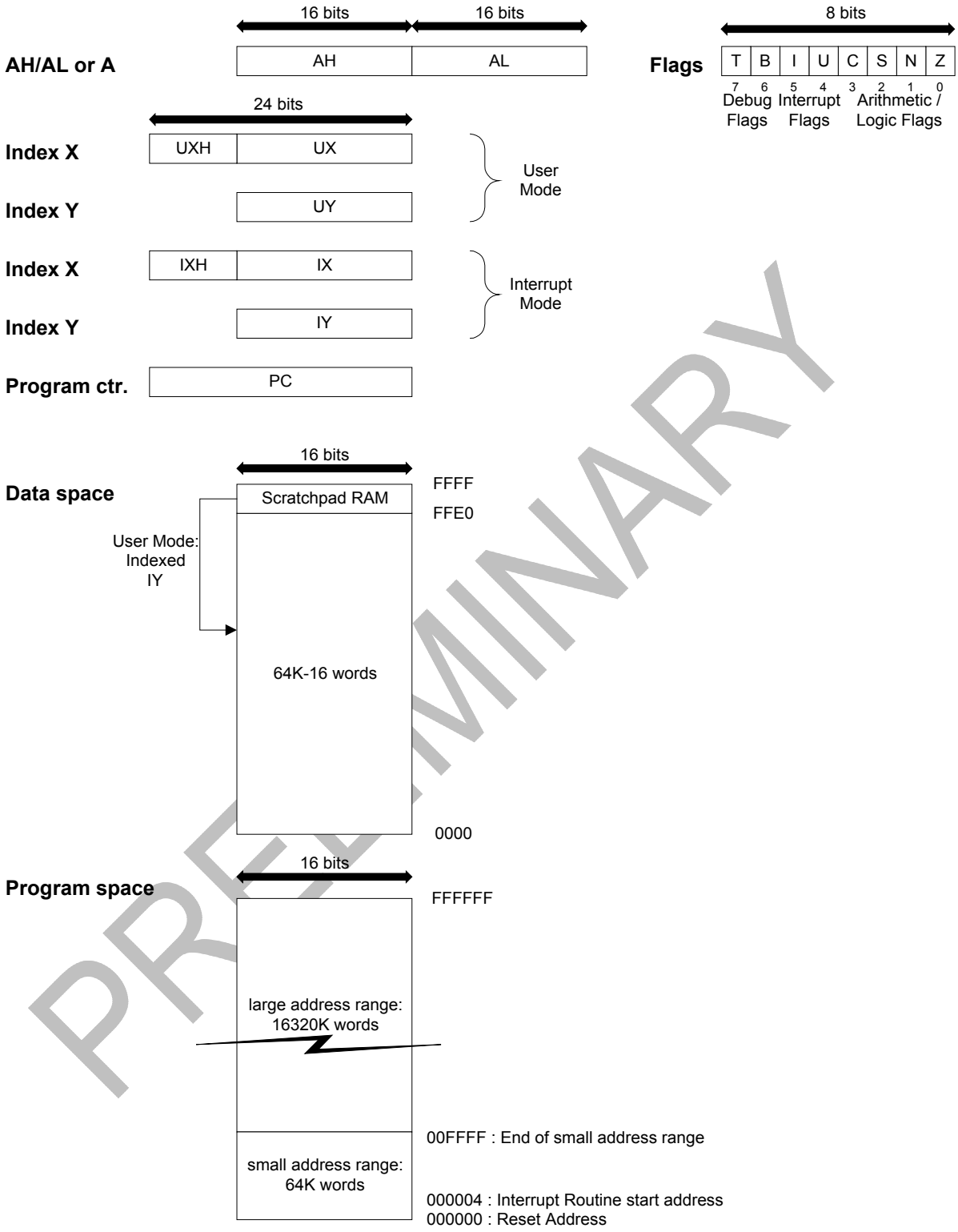
External Ports

- Peripherals are connected to multiple device pins.
- Each port has a unique multiplexing scheme to select port configuration.
- The number of 4-bit and 8-bit ports varies depending on the package and options.

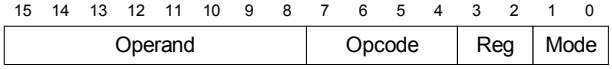
Power Supplies

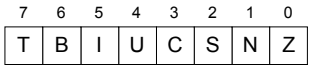
- 1.8V core supply.
- 3.3V I/O supply.
- On-chip power-on reset circuit.
- 5V tolerant I/O on ports B, K, L, N, P and Q.
- 2mA and 4mA output drive.

Programmer's Model



Instruction Set





Operand	*Opcode*	*Reg*	*Mode*	*Assembler*		*Operation*	*Flags*
not H'00	H'0	00	00	PREFIX	operand	ARG_EXT = (ARG_EXT<<8) + operand	-
H'00	H'0	00	00	NOP		None	-
H'00	H'0	01	00	BRK		Stop for debug	-
H'00	H'0	10	00	SLEEP		Enter sleep mode	-
H'00	H'0	11	00	SIF		Perform ESIF access during instruction	-
-	H'0	00	01	ST flags	@(<nn>,y)	@(<nn>,y)← flags	-
-	H'0	01	01	LD flags	@(<nn>,y)	flags ← @(<nn>,y)	ALL
-	H'0	11	01	RTI	@(<nn>,y)	PC ← {IXH, IX}; flags ← data	ALL
H'00	H'0	10	01	UNSIGNED		Operation modifier: unsigned	-
H'01	H'0	10	01	SIGNED		-	
H'FF	H'0	10	01	BC		for(AL; AL>0; AL--) @(Y++) ← @(X++)	-
H'FE	H'0	10	01	BRXL		PC ← PC + X[15:0] + 1. X[15:0] sign extended.	-
-	H'0	00	10	ST UX	@(<nn>,y)	@(<nn>,y) ← UX[15:0]	-
-	H'0	01	10	LD UX	@(<nn>,y)	UX[15:0] ← @(<nn>,y)	-
-	H'0	10	10	ST XH	@(<nn>,y)	@(<nn>,y) ← (U==1) ? UX[23:16] : {IX[23:16], UX[23:16]}	-
-	H'0	11	10	LD XH	@(<nn>,y)	(U==1) ? UX[23:16] : {IX[23:16], UX[23:16]} ← @(<nn>,y)	-
-	H'0	00	11	ST UY	@(<nn>,y)	@(<nn>,y) ← UY[15:0]	-
-	H'0	01	11	LD UY	@(<nn>,y)	UY[15:0] ← @(<nn>,y)	-
-	H'1	-	-	LD	reg, data	reg ← data	NZ
-	H'1	-	-	LD.B†	reg, data	reg[15:0] ← data[7:0] or data[15:8] – sign expended	NZ
-	H'1	-	-	LD.BU†	reg, data	reg[15:0]← data[7:0] or data[15:8] – zero extended	NZ
-	H'2	-	00	PRINT	reg, data	None. Debug request for simulators.	-
-	H'2	-	not-00	ST	reg, data	data ← reg	NZ
-	H'2	-	not-00	ST.B†	reg, data	data[7:0] ← reg[7:0]	NZ
				MOV	regd,AL	regd[15:0] ← AL[15:0]: regd == X, XH and Y	
				MOV	regx,AH	regx[15:0] ← AH[15:0]: regx == X, and XH	
				MOV	rega, Y	rega[15:0] ← Y[15:0]: rega == AH and AL	
				MOV24	X:,A	XH[7:0] ← AH[7:0], X[15:0] ← AL[15:0]	

Reg Register Access Field

Reg field	*reg*	*regd*	*regx*	*rega*
00	AH			AH
01	AL	XH	XH	AL
10	X	X	X	
11	Y	Y		

† Indicates UNSIGNED prefix instruction required for this instruction.
<nn> represents the instruction operand for instructions with a specific addressing mode.

Operand	*Opcode*	*Reg*	*Mode*	*Assembler*		*Operation*	*Flags*
-	H'3	-	-	ADD	reg, data	reg ← reg + data	CSNZ
-	H'4	-	-	ADDC	reg, data	reg ← reg + data + C	CSNZ
-	H'5	-	-	SUB	reg, data	reg ← reg – data	CSNZ
-	H'6	-	-	SUBC	reg, data	reg ← reg – data – C	CSNZ
-	H'7	-	-	NADD	reg, data	reg ← -reg + data	CSNZ
-	H'8	-	-	CMP	reg, data	flags ← reg – data	CSNZ
-	H'9	00	-	UMULT†	data	A ← AL * data	-
-	H'9	00	-	SMULT	data	Sign Extend. A ← AL * data	-
-	H'9	01	-	UDIV†	data	AL ← A ÷ data; AH ← rem	-
-	H'9	01	-	SDIV	data	Sign Extend. AL ← A ÷ data; AH ← rem	-
-	H'9	10	-	TST	data	flags ← data	NZ
-	H'9	11	-	BSR	addr	X ← PC + 1; PC ← branch_addr	-
-	H'A	00	-	ASL	data	C←[AH, AL]←0	C
-	H'A	00	-	LSL	data	C←[AH, AL]←0	C
-	H'A	01	-	ASR	data	AH[15]→[AH, AL]→C	C
-	H'A	01	-	LSR†	data	0→[AH,AL]→C	C
-	H'A	10	-	ROL	data	C←[AH,AL]←C	C
-	H'A	11	-	ROR	data	C→[AH,AL]→C	C
-	H'B	-	-	OR	reg, data	reg ← reg | data	NZ
-	H'C	-	-	AND	reg, data	reg ← reg & data	NZ
-	H'D	-	-	XOR	reg, data	reg ← reg ^ data	NZ
-	H'E	00	-	BRA	addr	PC ← branch_addr	-
-	H'E	01	-	BLT	addr	if S = 1 PC ← branch_addr	-
-	H'E	10	-	BPL	addr	if N = 0 PC ← branch_addr	-
-	H'E	11	-	BMI	addr	if N = 1 PC ← branch_addr	-
-	H'F	00	-	BNE	addr	if Z = 0 PC ← branch_addr	-
-	H'F	01	-	BEQ	addr	if Z = 1 PC ← branch_addr	-
-	H'F	10	-	BCC	addr	if C = 0 PC ← branch_addr	-
-	H'F	11	-	BCS	addr	if C = 1 PC ← branch_addr	-

Mode Field

mode	*Data Mode : source or destination*		*Address Mode: Branch Address*	
00	Immediate	data = 16-bit sign extended operand	PC relative	PC + 24-bit operand
01	Direct	data = 16-bit value @ 16-bit operand address	Direct	{XH, @ 16-bit operand address}
10	Indexed X	data = 16-bit value @ X+16-bit operand address	X Relative	{XH, X} + 24-bit sign extended operand
11	Indexed Y	data = 16-bit value @ Y+16-bit operand address	Indexed Y	{XH, @(Y + 16-bit operand)}

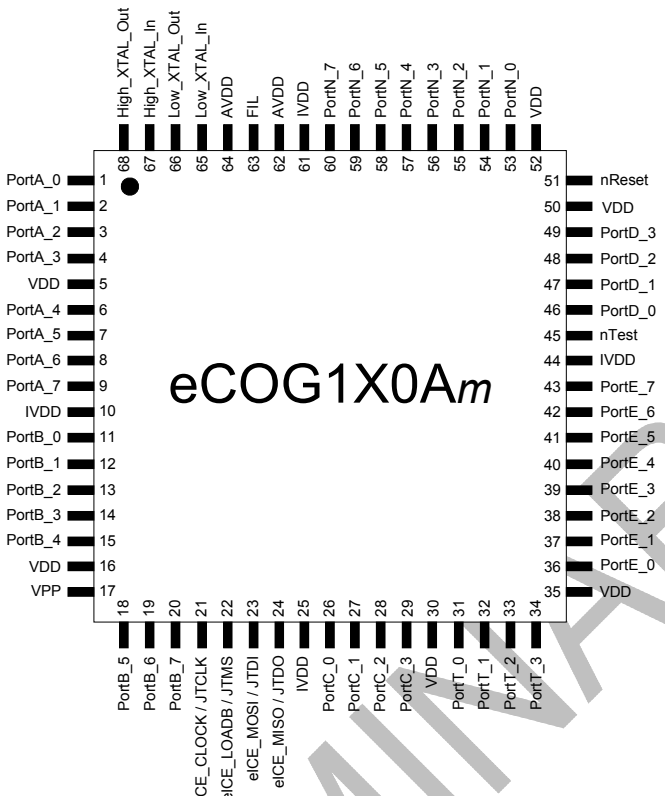
mode	*Data Mode Byte Accesses: source or destination*	
00	unused	
01	Direct	data = 8-bit value @ 17-bit operand byte address
10	Indexed X	data = 8-bit value @ 17-bit byte address in {XH,X}+17-bit operand byte address
11	Indexed Y	data = 8-bit value @ 16-bit word address in Y+17-bit operand byte address

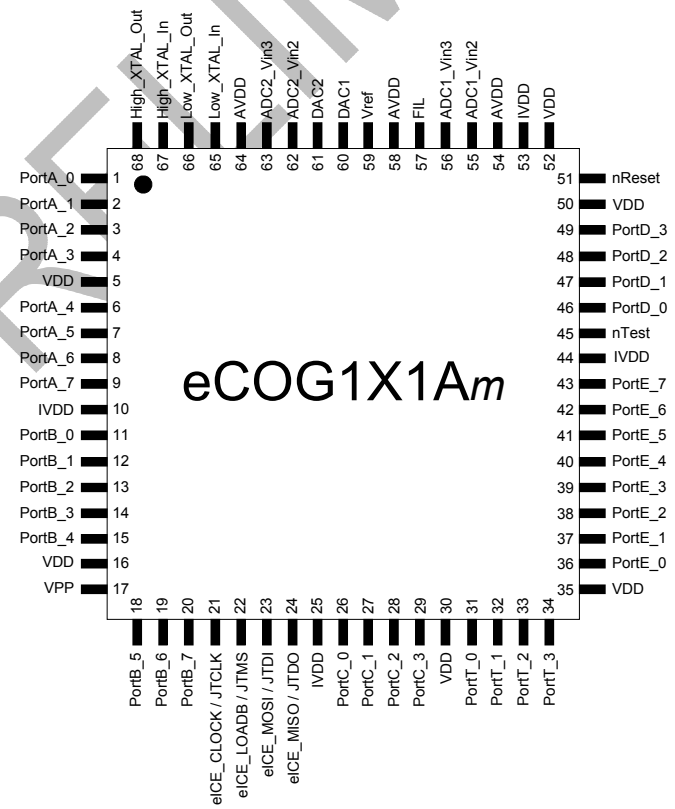
Table of eCOG1X variants

Product #	FLASH	ETH	USB	ADC	DAC	4 Bit Ports	8 Bit Ports	PACKAGE
eCOG1X0A1	128K					3	4	68 QFN
eCOG1X0A2	256K					3	4	68 QFN
eCOG1X0A5	512K					3	4	68 QFN
eCOG1X1A1	128K			4	2	3	3	68 QFN
eCOG1X1A2	256K			4	2	3	3	68 QFN
eCOG1X4A2	256K		Y			2	4	68 QFN
eCOG1X4A5	512K		Y			2	4	68 QFN
eCOG1X5A2	256K		Y	4	2	2	3	68 QFN
eCOG1X5A5	512K		Y	4	2	2	3	68 QFN
eCOG1X8A2	256K	Y				4	1	68 QFN
eCOG1X8A5	512K	Y				4	1	68 QFN
eCOG1X9A2	256K	Y		4	2	3	1	68 QFN
eCOG1X9A5	512K	Y		4	2	3	1	68 QFN
eCOG1X2B1	128K			11	2	7	4	100 QFN
eCOG1X2B2	256K			11	2	7	4	100 QFN
eCOG1X6B2	256K		Y	11	2	5	3	100 QFN
eCOG1X6B5	512K		Y	11	2	5	3	100 QFN
eCOG1X10B2	256K	Y		11	2	5	2	100 QFN
eCOG1X10B5	512K	Y		11	2	5	2	100 QFN
eCOG1X14B2	256K	Y	Y	11	2	4	2	100 QFN
eCOG1X14B5	512K	Y	Y	11	2	4	2	100 QFN
eCOG1X2Z1	128K			14	2	8	11	208 BGA
eCOG1X2Z2	256K			14	2	8	11	208 BGA
eCOG1X2Z5	512K			14	2	8	11	208 BGA
eCOG1X6Z2	256K		Y	14	2	8	11	208 BGA
eCOG1X6Z5	512K		Y	14	2	8	11	208 BGA
eCOG1X10Z2	256K	Y		14	2	8	11	208 BGA
eCOG1X10Z5	512K	Y		14	2	8	11	208 BGA
eCOG1X14Z2	256K	Y	Y	14	2	8	11	208 BGA
eCOG1X14Z5	512K	Y	Y	14	2	8	11	208 BGA

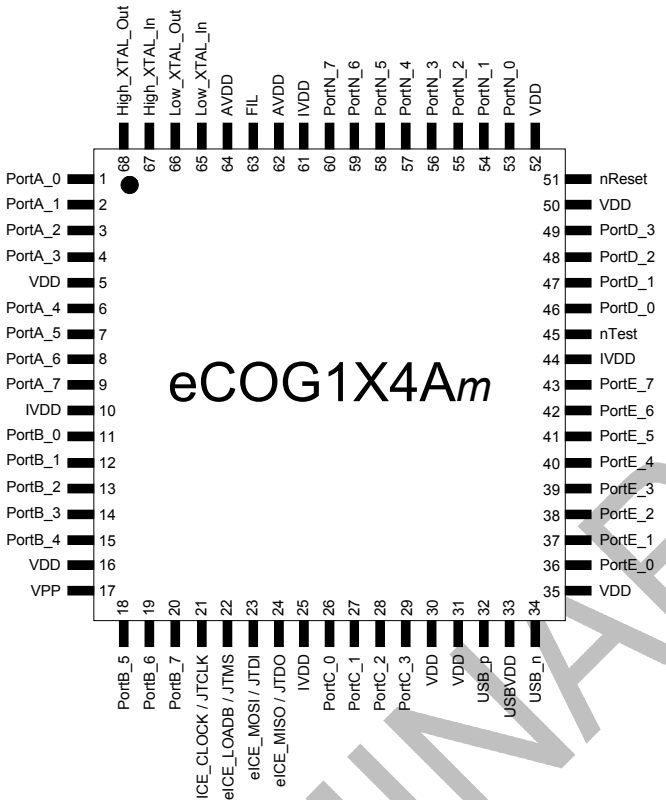
Package Outlines

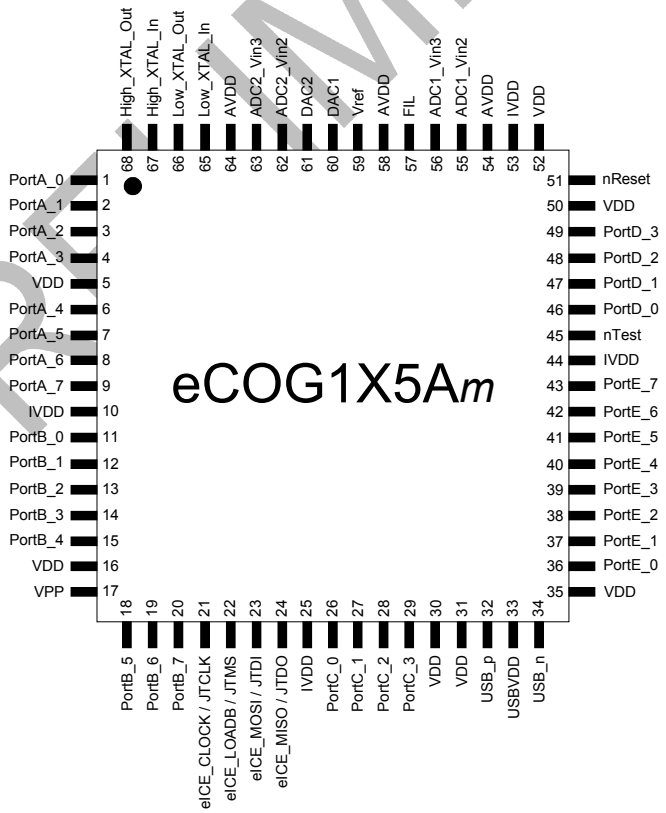
Top View



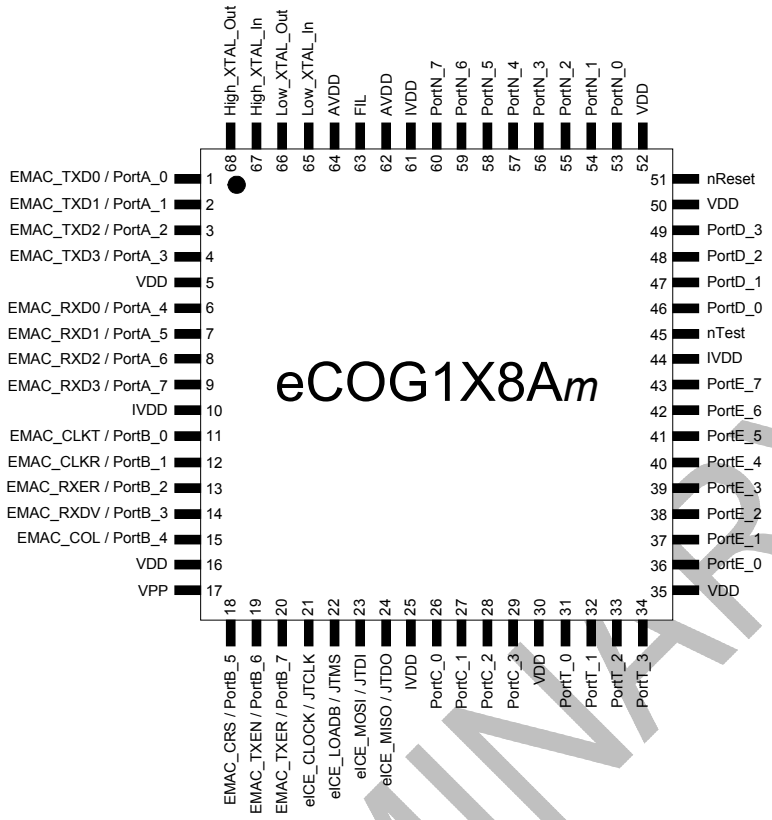


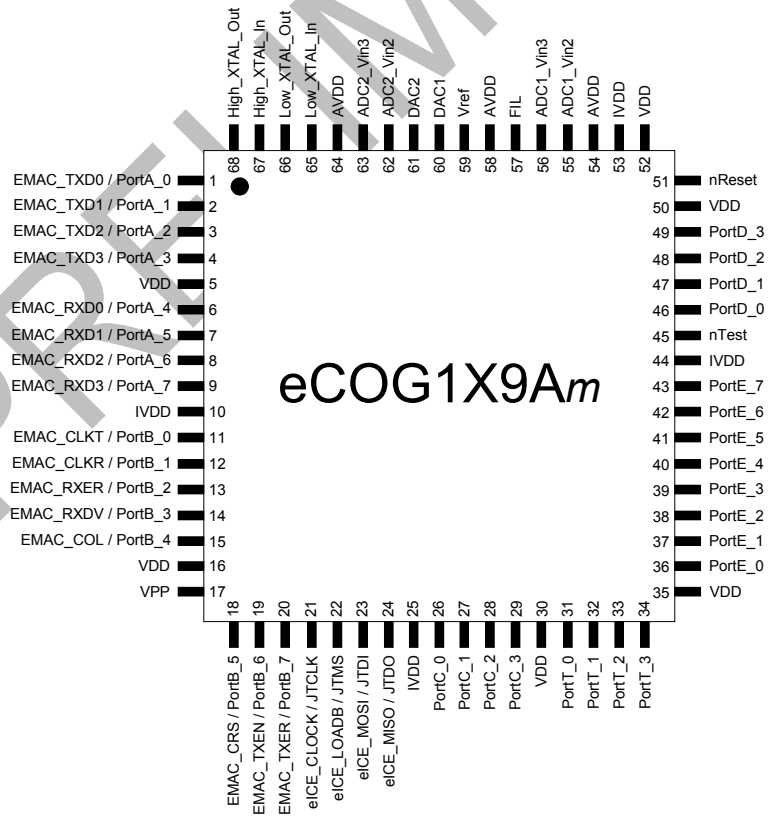
Top View



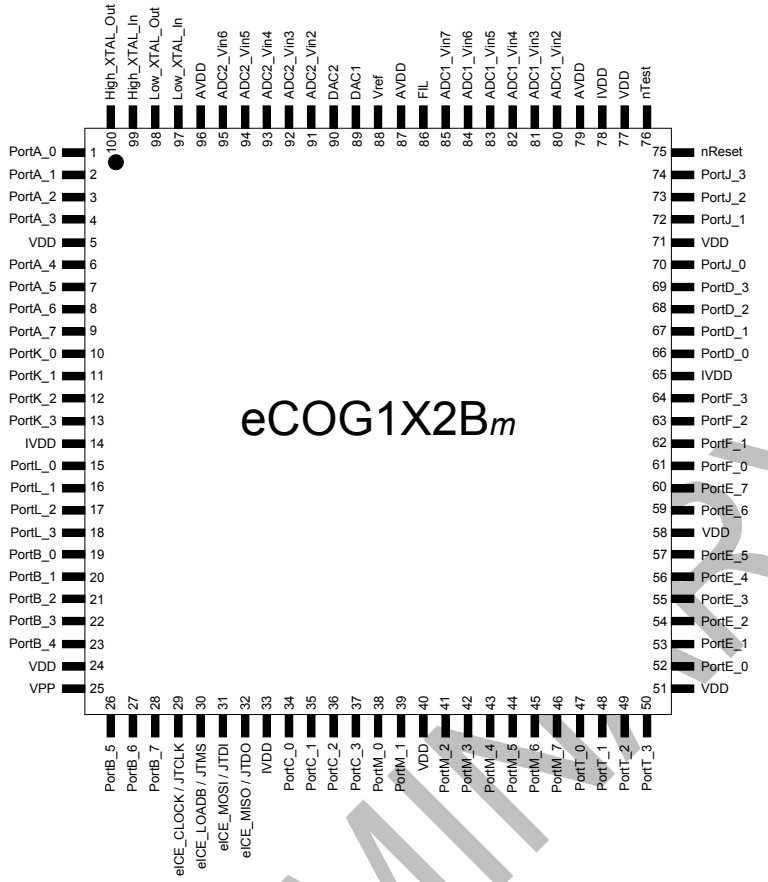


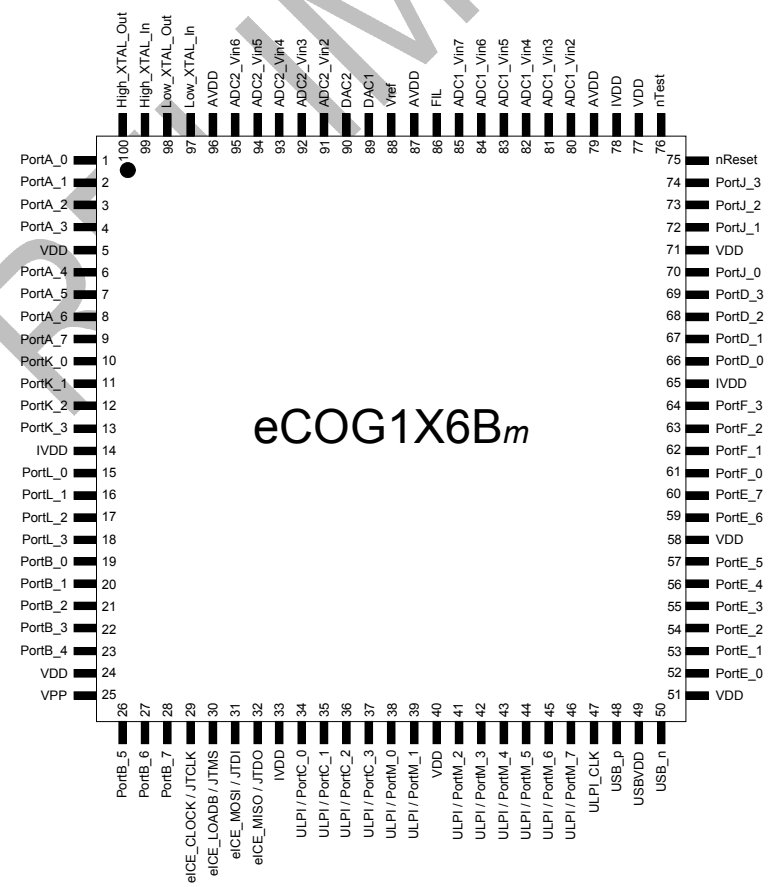
Top View



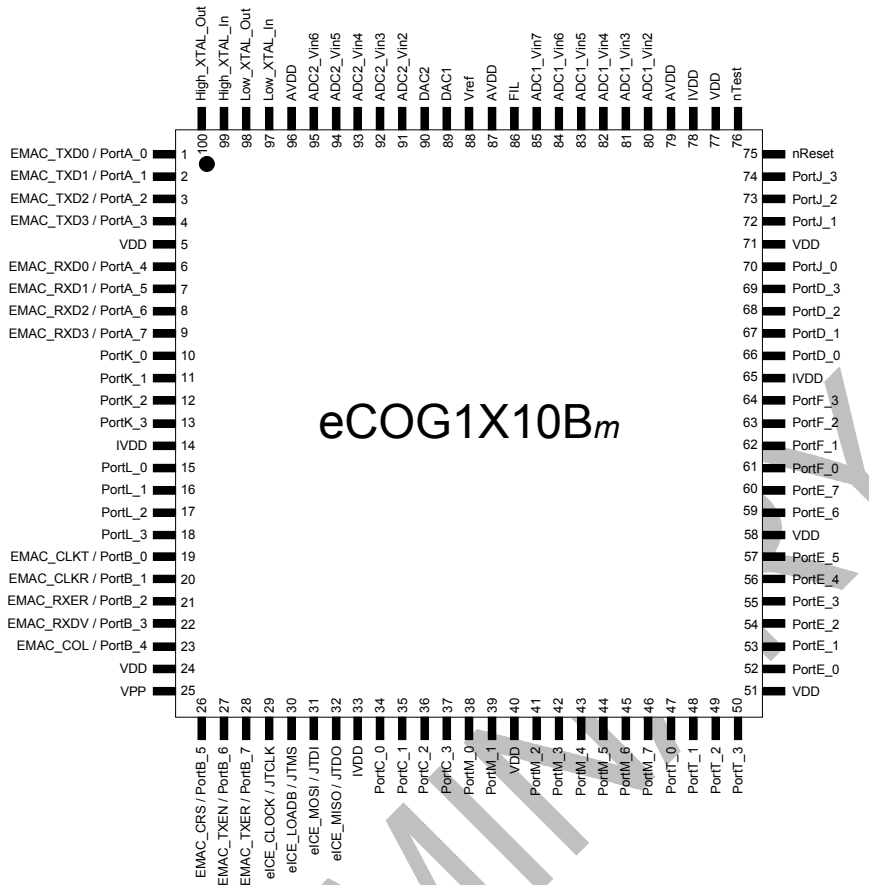


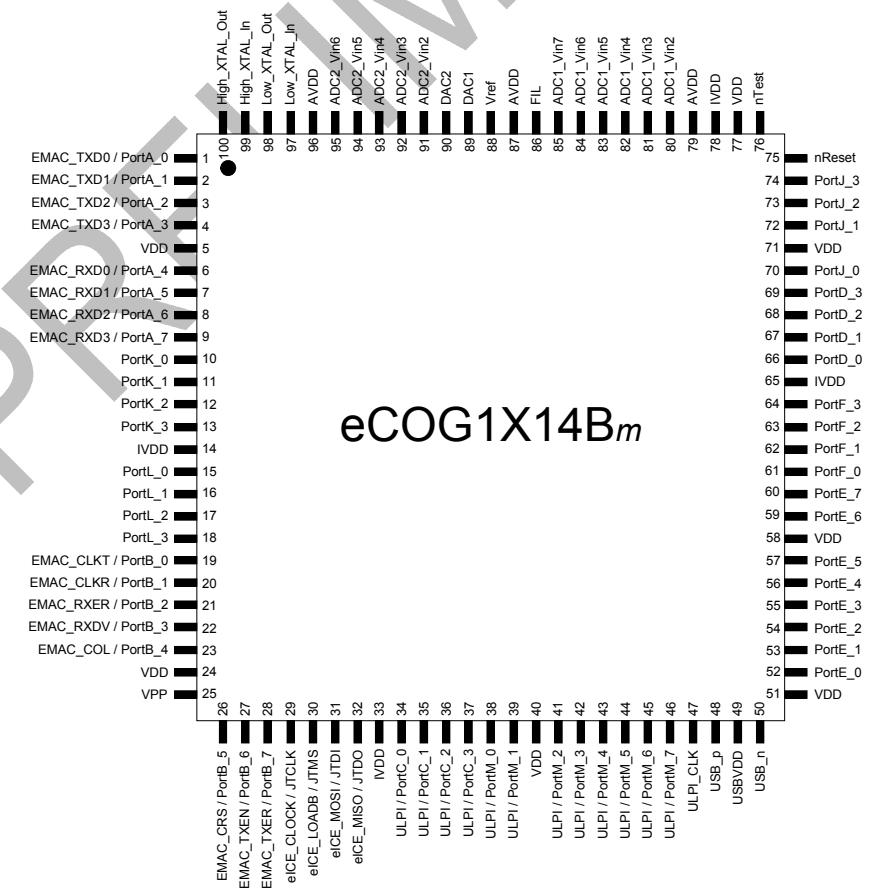
Top View



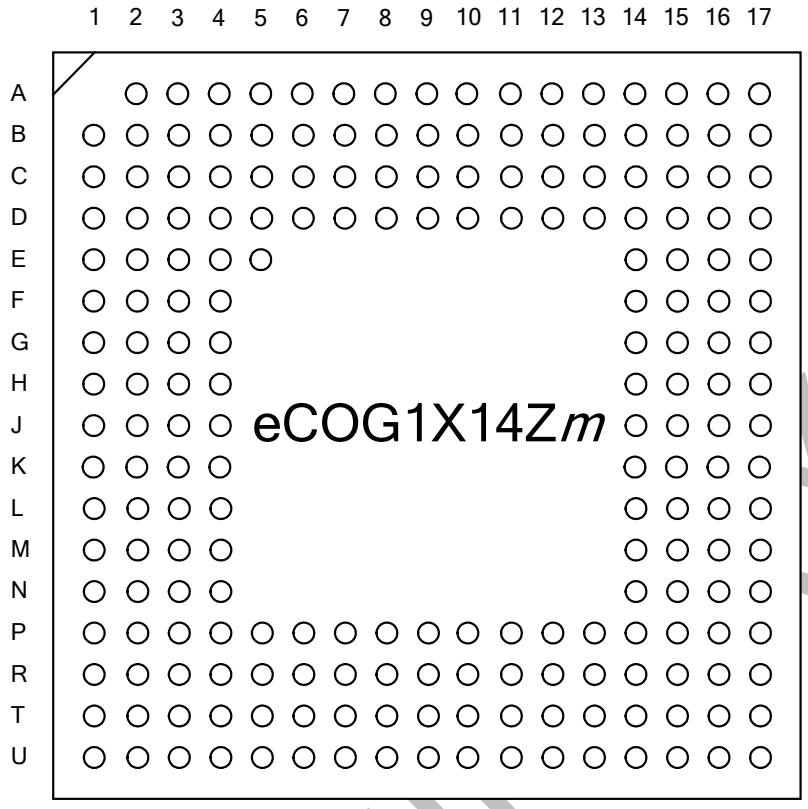


Top View





Top View



Pin	Description	Pin	Description	Pin	Description	Pin	Description
		B1	High_XTAL_Out	C1	NC	D1	EMAC_RXD0 / A_4
A2	Low_XTAL_Out	B2	AGND	C2	EMAC_TXD1 / A_1	D2	EMAC_TXD3 / A_3
A3	ADC2_Vin6	B3	Low_XTAL_In	C3	High_XTAL_In	D3	EMAC_TXD0 / A_0
A4	ADC2_Vin4	B4	ADC2_Vin5	C4	AVDD	D4	GND
A5	ADC2_Vin1	B5	ADC2_Vin2	C5	ADC2_Vin7	D5	GND
A6	DAC1	B6	DAC2	C6	ADC2_Vin3	D6	GND
A7	AGND	B7	Vref	C7	NC	D7	VDD
A8	ADC1_Vin7	B8	FIL	C8	AVDD	D8	GND
A9	ADC1_Vin6	B9	ADC1_Vin5	C9	ADC1_Vin2	D9	GND
A10	ADC1_Vin4	B10	ADC1_Vin3	C10	AVDD	D10	IVDD
A11	ADC1_Vin1	B11	AVDD	C11	Rext	D11	VDD
A12	NC	B12	NC	C12	PortN_6	D12	VDD
A13	PortN_7	B13	PortN_5	C13	PortN_3	D13	GND
A14	PortN_4	B14	PortN_2	C14	nTest	D14	GND
A15	PortN_1	B15	PortN_7	C15	nReset_out	D15	PortJ_3
A16	nReset_in	B16	PortJ_2	C16	PortJ_1	D16	PortD_2
A17	PortJ_0	B17	PortD_3	C17	PortD_1	D17	PortI_5
E1	EMAC_RXD2 / A_6	F1	PortK_1	G1	PortK_3	H1	PortP_2
E2	EMAC_RXD1 / A_5	F2	PortK_0	G2	PortK_2	H2	PortP_1
E3	EMAC_TXD2 / A_2	F3	EMAC_RXD3 / A_7	G3	PortP_0	H3	PortP_3
E4	GND	F4	GND	G4	VDD	H4	GND
E5	GND						
E14	GND	F14	IVDD	G14	VDD	H14	GND
E15	PortD_0	F15	PortI_6	G15	PortI_3	H15	PortH_1
E16	PortI_7	F16	PortI_4	G16	PortI_1	H16	PortH_6

Pin	Description	Pin	Description	Pin	Description	Pin	Description
E17	PortI_2	F17	PortI_0	G17	PortH_7	H17	PortH_5
J1	PortP_6	K1	PortQ_1	L1	PortQ_2	M1	PortQ_4
J2	PortP_5	K2	PortP_7	L2	PortQ_3	M2	PortQ_6
J3	PortP_4	K3	PortQ_0	L3	PortQ_5	M3	EMAC_CLKR / B_1
J4	GND	K4	IVDD	L4	GND	M4	GND
J14	GND	K14	IVDD	L14	GND	M14	GND
J15	PortH_0	K15	PortG_1	L15	PortF_3	M15	PortE_7
J16	PortH_4	K16	PortG_3	L16	PortG_0	M16	PortF_2
J17	PortH_3	K17	PortH_2	L17	PortG_2	M17	PortF_1
N1	PortQ_7						
N2	PortL_2						
N3	VPP						
N4	GND						
N14	VDD						
N15	PortE_2						
N16	PortE_6						
N17	PortF_0						
P1	PortL_0	R1	PortL_1	T1	PortL_3	U1	EMAC_TXEN / B_6
P2	EMAC_CLKT / B_0	R2	EMAC_RXER / B_2	T2	EMAC_CRS / B_5	U2	eICE_LOADB / JTMS
P3	EMAC_RXDV / B_3	R3	EMAC_COL / B_4	T3	eICE_CLOCK / JTCLK	U3	eICE_MOSI / JTDI
P4	GND	R4	EMAC_TXER / B_7	T4	PortR_0	U4	PortR_2
P5	GND	R5	eICE_MISO / JTDO	T5	PortR_1	U5	PortR_4
P6	VDD	R6	PortR_3	T6	PortR_5	U6	PortR_6
P7	GND	R7	PortR_7	T7	PortS_0	U7	PortS_1
P8	IVDD	R8	PortS_2	T8	PortS_3	U8	IVDD
P9	VDD	R9	PortS_6	T9	PortS_5	U9	PortS_4
P10	VDD	R10	ULPI_DATA1 / M_1	T10	ULPI_RST / C_0	U10	PortS_7
P11	VDD	R11	PortT_0	T11	ULPI_NXT / C_2	U11	ULPI_DIR / C_1
P12	VDD	R12	PortT_1	T12	ULPI_DATA2 / M_2	U12	ULPI_STOP / C_3
P13	GND	R13	USB_n	T13	ULPI_DATA3 / M_3	U13	ULPI_DATA0 / M_0
P14	GND	R14	USB_p	T14	ULPI_DATA6 / M_6	U14	ULPI_DATA4 / M_4
P15	PortT_2	R15	USBVDD	T15	ULPI_DATA7 / M_7	U15	ULPI_DATA5 / M_5
P16	PortE_4	R16	PortE_0	T16	GND	U16	PortT_3
P17	PortE_5	R17	PortE_3	T17	PortE_1	U17	ULPI_CLK

Notes:

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