

# **CHIP SPECIFICATION TCC8900**

**High Performance and Low-Power Processor  
For Digital Media Applications**

**Rev. 1.01**

**Aug 18, 2009**

***Telechips***



## Revision History

Date	Revision	Description
2008-12-05	0.00	* Initial Release
2008-12-11	0.01	* Swapping of EDIXD0 and EDIXD8 in the Pin Description * Swapping of EDIXD1 and EDIXD9 in the Pin Description * Swapping of EDIXD2 and EDIXD10 in the Pin Description * Swapping of EDIXD3 and EDIXD11 in the Pin Description
2008-12-29	0.02	* The ball maps of H1, J1, K1, L1, M1, N1, P1, T1, U1, V1, W1, Y1, L2, M2, N2, P2, R2, U2, V2, W2, Y2, N3, P3, R3, T3, U3, V3, W3, Y3, P4, R4, T4, U4, V4, W4, Y4, R5, T5, U5, V5, W5, Y5, P6, R6, V6, W6, Y6, P7, T7, U7, V7, Y7, T8, U8, V8, W8, Y8, P9, R9, V9, W9, Y9, P10, R10, W10, Y10, T13, T14, N17, N18, M20, N20, P20 were changed.
2009-01-22	0.03	The ball description on the Table 3.9 has been changed. - GPIOB[26] → G6 - GPIOB[27] → C11 - GPIOB[28] → G7 - GPIOB[29] → D10
2009-02-05	0.04	* The recommended operating frequency for each block was added.
2009-03-10	0.05	* The resolution of the ADC(TSADC) was changed from 10 bits to 12 bits.
2009-06-05	0.06	* The order of the TCO3 ~ TCO0 is changed to TCO0 ~ TCO3. * The initial states of the GPIO were changed.
2009-08-07	1.00	* Changing AC SPEC DAI(I2S) * The initial states of the GPIOs have been changed.
2009-08-18	1.01	* The ball map or pin description has been changed. * The value of Ccard for SDMMC has been changed from 50pF to 30pF. * Updating "Timing Parameters for Each Symbol"



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## **1 Introduction**

The TCC8900 is the system LSI for digital multimedia applications which based on ARM1176JZF-S, ARM's proprietary RISC CPU core. It can decode and encode various types of video and audio standards by software and dedicated hardware accelerators – JPEG / MPEG1 / MPEG2 / MPEG4-SP/ASP / H.264 / VC-1 / RV and other types of video standard and MP3 / AAC / MPEG4-AAC / MPEG4-BSAC and other types of standard for audio

The on-chip high speed USB2.0 device controller enables the data transmission between a personal computer and storage device such as NAND flash, HDD, CD, SD, MMC and Memory Stick etc, which can be controlled by the TCC8900.

## 1.1 TCC8900 Features

Table 1.1 TCC8900 Features

Category	Description
PROCESSORS (ARM1176JZF-S)	<ul style="list-style-type: none"> <li>* <b>TrustZone™</b> security extensions</li> <li>* High-speed <b>AMBA AXI</b> Bus Interface</li> <li>* High performance integer processor <ul style="list-style-type: none"> <li>* 8 stage pipelines</li> <li>* Separate load-store and arithmetic pipelines</li> <li>* Branch prediction with return stack</li> </ul> </li> <li>* Instruction and Data MMU(Memory Management Units) <ul style="list-style-type: none"> <li>* Micro TLB structures backed by a unified Main TLB.</li> </ul> </li> <li>* Virtually indexed and physically addressed caches</li> <li>* Level one TCM(Tightly-Coupled Memory) <ul style="list-style-type: none"> <li>* 16KBs ITCM and 16KBs DTCM</li> </ul> </li> <li>* 16KBs Instruction/Data Caches <ul style="list-style-type: none"> <li>* Including a non-blocking data cache with Hit-Under-Miss(HUM)</li> </ul> </li> <li>* <b>Vector-Floating-Point(VFP)</b> coprocessor support</li> <li>* ARM Jazelle technology for efficient embedded Java execution</li> <li>* JTAG interface for code debugging</li> </ul>
MEMORY ORGANIZATION <sup>1</sup>	<ul style="list-style-type: none"> <li>* Internal(On-Chip) Memory <ul style="list-style-type: none"> <li>* 16KB Boot-ROM (EHI, NAND, USB Boot with security and etc.)</li> <li>* 16KB Internal SRAM (Shared by Hardware)</li> </ul> </li> <li>* External(Off-Chip) Memory <ul style="list-style-type: none"> <li>* SDRAM : up to 200MHz</li> <li>* mDDR SDRAM : up to 200MHz(400Mbps)</li> <li>* DDR SDRAM : up to 200MHz(400Mbps)</li> <li>* DDR2 SDRAM : up to 400MHz(800Mbps)</li> <li>* 32bits Data Bus</li> </ul> </li> </ul>
VIDEO CODEC	<ul style="list-style-type: none"> <li>* <b>Decompressor<sup>2</sup> (Decoder) – up to 30fps @ Full-HD (1920x1080)</b> <ul style="list-style-type: none"> <li>* H.263 : up to 40Mbps</li> <li>* MPEG 1/2 <ul style="list-style-type: none"> <li>* Up to Main Profile @ High Level</li> <li>* Max. bitrate : up to 40Mbps</li> </ul> </li> <li>* MPEG4-ASP <ul style="list-style-type: none"> <li>* Up to Advanced Simple Profile Including DivX3.x</li> <li>* Max. bitrate : up to 35Mbps</li> </ul> </li> <li>* MPEG4-AVC(H.264) <ul style="list-style-type: none"> <li>* Up to High Profile @ Level 5.1<sup>3</sup></li> <li>* Max. bitrate : up to 25Mbps</li> </ul> </li> <li>* VC-1 <ul style="list-style-type: none"> <li>* Up to Advanced Profile @ Level 3.0</li> <li>* Max. bitrate : up to 30Mbps</li> </ul> </li> <li>* RV <ul style="list-style-type: none"> <li>* Real Video 10 ( Backward Compatible for RV8.9)</li> <li>* Max. bitrate : up to 30Mbps</li> </ul> </li> <li>* JPEG : up to 12Mpixels</li> </ul> </li> <li>* <b>Compressor<sup>4</sup> (Encoder) – up to 30fps or 24fps @HD(1280x720)</b> <ul style="list-style-type: none"> <li>* H.263: up to 30fps @ HD(1280x720p)</li> <li>* MPEG4-ASP : up to 30fps @ HD(1280x720p)</li> <li>* H.264: up to 24fps @ HD(1280x720p)</li> <li>* JPEG: up to 12Mpixels</li> </ul> </li> </ul>
GRAPHIC ENGINE	<ul style="list-style-type: none"> <li>* <b>2D/3D Graphic</b> <ul style="list-style-type: none"> <li>* High Geometry and Pixel Processing</li> <li>* Up to 7M polygon<sup>5</sup></li> <li>* Full OpenVG v1.1 Support <ul style="list-style-type: none"> <li>* Lines, Squares, Triangles, Points</li> </ul> </li> <li>* Vector Graphics</li> <li>* ROP 3/4</li> <li>* Arbitrary Rotation / Scaling</li> <li>* Alpha Blending</li> </ul> </li> </ul>

<sup>1</sup> The maximum operation frequency can be limited by the system configuration.

<sup>2</sup> The performance of the video decoding can be limited by the system configuration.

<sup>3</sup> Up to 1920x1080 30fps 25Mbps : Ref.Frame : 96Mbyte for VPU Memory in case of 32 Ref frame

<sup>4</sup> The performance of the video encoding can be varied by the system configuration.

<sup>5</sup> The maximum performance for this can be varied by the system configuration.

	<ul style="list-style-type: none"> <li>* Multitexture BitBLT</li> <li>* Full OpenGL ES v2.0, v1.x Support</li> <li>* 4X /16X FSAA</li> <li>* Flat/Gouraud Shading</li> <li>* Perspective Correct Texturing</li> <li>* Point Sampling/Bilinear/Trilinear Filtering</li> <li>* Mipmapping</li> <li>* Multi Texturing</li> <li>* Dot3 Bump Mapping</li> <li>* Alpha Blending</li> <li>* Stencil Buffering (4-bit)</li> <li>* JSR 184</li> <li>* Point Sprites</li> <li>* 2 bit per pixel Texture Compressing (FLXTC)</li> <li>* 4 bit per pixel Texture Compressing (ETC)</li> <li>* <b>Overlay Mixer</b> <ul style="list-style-type: none"> <li>* 8bpp (RGB332)</li> <li>* RGB (444, 454, 555, 565, 666, 888)</li> <li>* Alpha-RGB (444, 454, 555, 666, 888)</li> <li>* Sequential YUV (444, 422)</li> <li>* Separated YUV (444, 440, 422, 420, 411, 410)</li> <li>* Interleaved YUV (422, 420)</li> <li>* BitBLT (16 Raster Operations)</li> <li>* 3 Channel Source Mirror/Flip/90° , 180° , 270° Rotate</li> <li>* 1 Channel Destination Mirror/Flip/90° , 180° , 270° Rotate</li> <li>* 3 Channel Arithmetic Operation</li> <li>* 3 Channel YCbCr-to-RGB Color Space Converting</li> <li>* Overlay and Alphablending (2 overlay, 256-level alphablending)</li> <li>* Color LUT</li> <li>* Dithering</li> </ul> </li> </ul>
IMAGE ENHANCEMENT	<ul style="list-style-type: none"> <li>* <b>Histogram Measurement</b> <ul style="list-style-type: none"> <li>* Analyze the Luminance Components</li> <li>* Multi-frames Average Mode</li> <li>* User-defined Pixel Segments Support</li> </ul> </li> <li>* <b>Contrast Enhancement</b> <ul style="list-style-type: none"> <li>* User-defined Scaling Segments</li> <li>* Multi-frames Average Mode</li> </ul> </li> <li>* <b>De-Interlacer</b> <ul style="list-style-type: none"> <li>* Motion-adaptive and Pixel-based Processing</li> <li>* Film-mode Detection</li> <li>* Simple Edge-oriented Mode</li> <li>* Advanced Spatial-Temporal Mode</li> </ul> </li> <li>* <b>Noise Reduction</b> <ul style="list-style-type: none"> <li>* Directional-Smoothing Filter</li> <li>* Temporal-Recursive Filter</li> <li>* Noise Estimation</li> </ul> </li> <li>* <b>Sharpness</b> <ul style="list-style-type: none"> <li>* Spatial High-pass Filter</li> </ul> </li> </ul>
VIDEO IN/OUT	<ul style="list-style-type: none"> <li>* <b>Video Output</b> <ul style="list-style-type: none"> <li>* 2 Display Controllers <ul style="list-style-type: none"> <li>* Controller 0 has single image channel</li> <li>* Controller 1 has 3 image channels</li> </ul> </li> <li>* Progressive or Interlaced Digital Video Output</li> </ul> </li> <li>* <b>Supported Functions</b> <ul style="list-style-type: none"> <li>* 3 Channel Overlay / Chroma-Keying / Alpha-blending – Only for Controller 1</li> <li>* Gamma Correction</li> <li>* Look-up table for Indexed or RGB Color</li> <li>* Contrast, Brightness, Hue Function Supported.</li> </ul> </li> <li>* <b>Supported Output Media</b> <ul style="list-style-type: none"> <li>* TFT-LCD Supported</li> <li>* HDMI Output Supported : up to 1920x1080p</li> <li>* LVDS Output Supported : up to 1280x720p</li> <li>* Composite TV-Out ( NTSC/PAL )</li> </ul> </li> <li>* <b>Dual-Display Supported<sup>1</sup></b> <ul style="list-style-type: none"> <li>* Two types of supported media</li> </ul> </li> <li>* CPU Type Main/Sub LCD : Time Shared</li> </ul>

<sup>1</sup> The maximum resolution and combination of image channels can be determined by the system configuration

	<ul style="list-style-type: none"> <li>* <b>Video Input</b> <ul style="list-style-type: none"> <li>* CCIR-601/656 Interface</li> <li>* Camera Input Supported</li> <li>* 1 Channel Overlay / Chroma-Keying</li> <li>* Input Image Scaler – Output resolution is up to 4080x4080</li> </ul> </li> </ul>
SPECIAL HARDWARE	<ul style="list-style-type: none"> <li>* <b>DVB-H MPE-FEC</b></li> <li>* <b>ECC Controller</b></li> <li>* <b>Touch Screen Interface</b> <ul style="list-style-type: none"> <li>* 10/12 bits 8CH ADC</li> </ul> </li> </ul>
AUDIO	<ul style="list-style-type: none"> <li>* I2S Master &amp; Slave Interface <ul style="list-style-type: none"> <li>* 7.1 Channel Supported</li> </ul> </li> <li>* SPDIF Transmitter/Receiver <ul style="list-style-type: none"> <li>* 5.1 Channel Supported</li> </ul> </li> <li>* CD I/F</li> <li>* I2S Slave Interface</li> </ul>
STORAGE INTERFACE	<ul style="list-style-type: none"> <li>* USB 2 Channel Interface <ul style="list-style-type: none"> <li>* 1 Channel for USB 2.0 OTG</li> <li>* 1 Channel for USB1.1 Host</li> </ul> </li> <li>* UDMA 33/66, PIO Mode</li> <li>* NAND Flash Interface <ul style="list-style-type: none"> <li>* 8 Bits / 16 Bits</li> <li>* 4 CS Supported</li> </ul> </li> <li>* SD/MMC Controller : SD, MMC, SDIO, Ce-ATA</li> <li>* Memory Stick Pro/Pro-HG Supported</li> <li>* S-ATA Host <ul style="list-style-type: none"> <li>* Generation 1 : 1.5Gbps</li> <li>* Generation 2 : 3.0Gbps</li> </ul> </li> </ul>
HOST INTERFACE	<ul style="list-style-type: none"> <li>* EHI(External Host Interface) <ul style="list-style-type: none"> <li>* 8, 16bits, 18bits</li> <li>* 2 Channels</li> <li>* Bypass to LCD Port (CPU Type)</li> </ul> </li> </ul>
STREAMING INTERFACE	<ul style="list-style-type: none"> <li>* <b>TS Interface</b> <ul style="list-style-type: none"> <li>* 2 Channel TS serial interfaces shared by GPSB</li> <li>* 2 Channel TS parallel interfaces</li> </ul> </li> </ul>
PERIPHERALS	<ul style="list-style-type: none"> <li>* <b>UART</b> – up to 6 Channels</li> <li>* I2C ( 2 Master and 1 Slave ) – 2 Channels</li> <li>* <b>GPSB</b>(General Purpose Serial-Bus – Master/Slave) – 6 Channels <ul style="list-style-type: none"> <li>* Serial TS Interface Supported (Receiver Only) for <b>2 channels</b></li> </ul> </li> <li>* <b>CAN – Protocol 2.0 Supported</b></li> <li>* <b>Infra-Red Remote Receiver</b></li> <li>* <b>Timers</b> <ul style="list-style-type: none"> <li>* Four 16-bit timers with PWM output/counters</li> <li>* Two 20-bit timers</li> <li>* One 32-bit timer</li> </ul> </li> <li>* <b>DMA</b> - 12 Channels</li> <li>* <b>ADC</b> <ul style="list-style-type: none"> <li>* 8-Channel General purpose 12-bit</li> <li>* Shared by Touch Screen Controller</li> </ul> </li> </ul>
PMU	<ul style="list-style-type: none"> <li>* <b>RTC</b> : Power-Down Mode &amp; Auto-wakeup</li> <li>* Internal power island for saving the current consumption.</li> </ul>
PROCESS	<ul style="list-style-type: none"> <li>* 65nm CMOS</li> </ul>

## 1.2 Applications

Category	Description
Mobile Application Processor	<ul style="list-style-type: none"><li>* Smart-Phone Application</li><li>* Support of all the Mobile / Digital broadcasting services<ul style="list-style-type: none"><li>* T-DMB/S-DMB/DVB-H/ CMMB / ATSC-MH</li><li>* DVB-T / DTTB</li></ul></li><li>* Support of Touch Screen Controller</li><li>* Low-power consumption for power-down mode</li></ul>
Mobile Co-processor	<ul style="list-style-type: none"><li>* Mobile-TV Solution</li><li>* Mobile Multimedia Co-Processor</li></ul>
Portable Devices	<ul style="list-style-type: none"><li>* High quality Multimedia Player</li><li>* Low cost PDA application</li><li>* Multimedia Host Player</li></ul>
Portable Navigation	<ul style="list-style-type: none"><li>* 2D/3D Navigation</li><li>* Navigation with A/V System and D-TV</li></ul>
CAR	<ul style="list-style-type: none"><li>* Car Navigator<ul style="list-style-type: none"><li>- Multimedia Play</li></ul></li><li>* Multimedia Host Player<ul style="list-style-type: none"><li>- USB1.1 Host</li></ul></li></ul>

### 1.3 Block Diagram

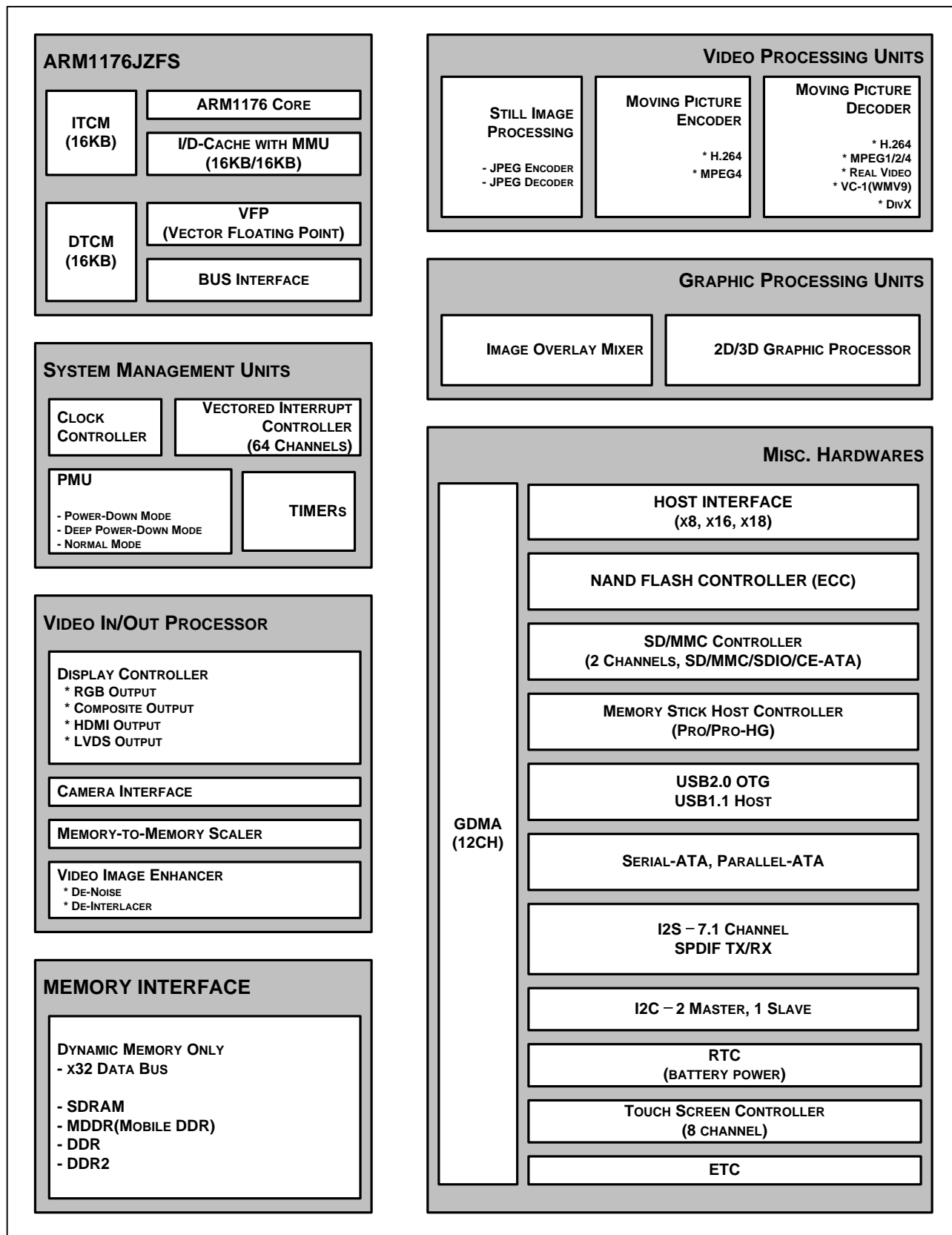


Figure 1.1 TCC8900 Functional Block Diagram

## 2 Hardware Features

Table 2.1 ARM1176JZFS Processor

ARM1176JZFS <sup>1</sup>	Key Features
Cache Organizations	<ul style="list-style-type: none"> <li>* 16KBs/16KBs I/D Caches</li> <li>* I/D MMU Supported</li> <li>* Java Accelerator</li> </ul>
Tightly Coupled Memory	<ul style="list-style-type: none"> <li>* 16KB Instruction TCM</li> <li>* 16KB Data TCM</li> </ul>
Debug Interface	* JTAG Synchronized Ports with RTCK

Memory Map	Description
0x00000000	Remapped Area <ul style="list-style-type: none"> <li>* REMAP = 00b : Boot-ROM</li> <li>* REMAP = 01b : Internal SRAM</li> <li>* REMAP = 10b : External SDRAM</li> <li>* REMAP = 11b : No-Remap</li> </ul>
0x10000000	Internal SRAM <ul style="list-style-type: none"> <li>* 16KBs Size</li> </ul>
0x20000000	Reserved for TLB for virtual MMU Table <ul style="list-style-type: none"> <li>* Do not use this area</li> </ul>
0x40000000 ~ 0x80000000	External SDRAM <ul style="list-style-type: none"> <li>* Up to 1GBs<sup>2</sup></li> </ul>
0xE0000000	Boot-ROM <ul style="list-style-type: none"> <li>* 16KBs size</li> </ul>
0xF0000000	Special Function Registers <ul style="list-style-type: none"> <li>* Hardware Control Registers</li> </ul>

Figure 2.1 Memory Organization

<sup>1</sup> If more detailed information is required, refer to the ARM1176JZFS Technical Reference Manual on ARM site.

<sup>2</sup> The maximum size for external SDRAM is determined by the system configuration and the size of external SDRAM.

Table 2.2 Video Controller

Video Codec	Key Features
Encoder	<ul style="list-style-type: none"> <li>* H.264 Encoding <ul style="list-style-type: none"> <li>- 24fps @ HD Resolution (1280x720p)</li> </ul> </li> <li>* MPEG-4-ASP Encoding <ul style="list-style-type: none"> <li>- 30fps @ HD Resolution (1280x720p)</li> </ul> </li> <li>* H.263 Encoding <ul style="list-style-type: none"> <li>- 30fps @ HD Resolution (1280x720p)</li> </ul> </li> </ul>
Decoder	<ul style="list-style-type: none"> <li>* H.264 Decoding <ul style="list-style-type: none"> <li>- 30fps @ Full-HD Resolution</li> </ul> </li> <li>* MPEG4-ASP Decoding <ul style="list-style-type: none"> <li>- 30fps @ Full-HD Resolution</li> </ul> </li> <li>* H.263 Decoding <ul style="list-style-type: none"> <li>- 30fps @ Full-HD Resolution</li> </ul> </li> <li>* VC-1 Decoding <ul style="list-style-type: none"> <li>- 30fps @ Full-HD Resolution</li> </ul> </li> <li>* RV Decoding <ul style="list-style-type: none"> <li>- 30fps @ Full-HD Resolution</li> </ul> </li> </ul>

Table 2.3 Camera Interface

CAMERA I/F	Key Features
Various Input Formats	<ul style="list-style-type: none"> <li>* CCIR601/656 4:2:2</li> <li>* Down Scaling for Preview Display : 1/2, 1/4, 1/8</li> <li>* Change the Image size and windowing.</li> <li>* Support the master clock for camera module.</li> </ul>
Hardware Format Converter	<ul style="list-style-type: none"> <li>* Reconfigurable Packing the Pixel Data</li> <li>* Dispatching the Pixel Data into Y/Cb/Cr</li> <li>* Horizontal and Vertical Window Clipping</li> <li>* Overlaying the Background Frame for Still or Moving Pictures <ul style="list-style-type: none"> <li>→ Chroma-Keying</li> <li>→ Alpha-blending (0%, 25%, 50%, 75%, 100%, XOR)</li> </ul> </li> <li>* Support the Master Clock for Camera Module → w/o External Oscillator</li> </ul>
Maximum Resolutions	* up to 120MHz <sup>1</sup> for Still Image <sup>2</sup>

<sup>1</sup> The maximum frequency can be limited by the timing specification of the camera sensor or external device.

<sup>2</sup> The maximum resolution can be limited by the system configuration.



Table 2.4 Video Output Interface

Video Output Interface	Key Features
Color TFT LCD	<ul style="list-style-type: none"> <li>* Various type image sources → RGB565, RGB555, <b>RGB666</b>, RGB24, YCbCr4:2:0, YCbCr4:2:2</li> <li>* Various type YCbCr4:2:0 and YCbCr4:2:2 to RGB converter</li> <li>* Parallel <b>24bits</b> and 18bits pixel data output</li> <li>* 6(R):6(G):6(B)bits and 8(R):8(G):8(B)bits pixel data output</li> </ul>
Mono/Color STN LCD	<ul style="list-style-type: none"> <li>* Mono: 1, 2, 4bpp image source</li> <li>* Color: 8(332), 12(444), 555, 565 bpp image source</li> <li>* 4 and 8-bit pixel data interface</li> </ul>
NTSC/PAL Encoder Interface	<ul style="list-style-type: none"> <li>* CCIR601/656 interlace/non-interlace</li> <li>* RGB to YCbCr4:2:2 converter</li> </ul>
NTSC/PAL composite output	<ul style="list-style-type: none"> <li>* Supports all NTSC and PAL formats (NTSC-M/4.43, PAL-B/D/G/H/I/M/N/Combination N)</li> </ul>
HDMI Output <sup>1</sup>	<ul style="list-style-type: none"> <li>* The supported formats are <ul style="list-style-type: none"> <li>- 1920x1080p @ 60Hz</li> <li>- 1920x1080i @ 30Hz</li> <li>- 1280x720p @ 30Hz</li> <li>- 720x480i @ 60Hz</li> <li>- 720x480p @ 60Hz</li> <li>- etc.</li> </ul> </li> </ul>
LVDS Output	<ul style="list-style-type: none"> <li>* 5 Differential Data Lanes</li> <li>* Each data in each lane can be mapped to any pixel data and sync signals.</li> </ul>
Image Processing	<ul style="list-style-type: none"> <li>* OSD/Overlay: can mix up to 3 image sources. <ul style="list-style-type: none"> <li>- Channel 0 can't mix up for only 1 image channel</li> <li>- Channel 1 has the 3 overlay channels.</li> <li>- Chroma-keying</li> <li>- <b>256 level</b> Alpha-blending</li> <li>- Contrast/Brightness/Hue Control</li> <li>- Simple Gamma Correction Supported</li> <li>- LUT for each image channels</li> </ul> </li> <li>* Virtual Window: Panning / Sliding the Window</li> <li>* Subsampling: 1/2, 1/3, 1/4, 1/8</li> <li>* Duplication: x2, x3, x4, x8</li> </ul>

<sup>1</sup> The maximum resolution can be limited by the system configuration.

Table 2.5 DAI/CDIF Controller

I2S (DAI/CDIF)	Key Features
DAI (Digital Audio Interface)	<ul style="list-style-type: none"> <li>* System clock: 256fs, 384fs, 512fs.</li> <li>* Maximum 7.1 channel supported</li> <li>* Support of Master/Slave Mode with Reconfigurable Clock Polarity</li> <li>* Wide Range of Sampling Frequency in Audio application : 8kHz, 16kHz, 11.05kHz, 24kHz, 32kHz 44.1kHz, 48kHz</li> <li>* Supports the I2S (MSB Justified Mode )</li> <li>* Controls the Digital Audio Volume over the range 0dB to -90dB</li> <li>* Using 2 Double Buffers for Audio I/O Data</li> </ul>
CDIF (CD Interface)	<ul style="list-style-type: none"> <li>* CD Interface for Feasible Implementation of CD Application</li> <li>* Slave Mode</li> <li>* I2S (LSB Justified Mode)</li> </ul>

Table 2.6 SPDIF Controller

SPDIF	Key Features
General Features	<ul style="list-style-type: none"> <li>* Transmitter/Receiver Included</li> <li>* Bit Rate is 64 times the sampling frequency</li> <li>* Configurable 16/24 Bits Mode</li> </ul>
Maximum Operating Frequency	<ul style="list-style-type: none"> <li>* 24MHz Output Data-Rate</li> <li>→ SPDIF Clock = 12.288MHz, Ratio = 1</li> <li>→ 3.072Mbps / 48kHz (Data Rate)</li> </ul>

Table 2.7 External Device Interface

External Device Interface	Key Features
Static Memory Controller	<ul style="list-style-type: none"> <li>* Support of 4 Types Static Memory (NAND/IDE/ROM/SRAM)</li> <li>* Controllable Setup / Pulse Width / Hold Time</li> <li>* 8/16 Bits Width</li> </ul>

Table 2.8 USB 1.1 Host

USB 1.1 Host	Key Features
General Features	<ul style="list-style-type: none"> <li>* USB1.1 Host Compatible</li> <li>* OHCI 1.0 Compliant</li> <li>* 2 Down Stream Port <ul style="list-style-type: none"> <li>- 1 for Dedicated USB1.1 Host Port</li> <li>- 1 for nanoPHY for USB 2.0 OTG Port</li> </ul> </li> </ul>
PHY Interface	* On-Chip UTMI PHY Serial Interface
Maximum Operating Frequency	* 48MHz

Table 2.9 USB 2.0 OTG(On-The-GO)

USB 2.0 OTG	Key Features
General Feature	<ul style="list-style-type: none"> <li>* Compliant USB2.0 Specification</li> <li>* Support Interrupt, Bulk Transfer</li> <li>* Support FS/HS dual mode operation</li> <li>* 16bit interface</li> <li>* FIFO size configuration</li> </ul>
USB DMA	<ul style="list-style-type: none"> <li>* 3 Channel DMA (EP1,EP2,EP3)</li> <li>* Support 16/32bit MCU interface</li> <li>* Single / Fly mode</li> <li>* 4x32 FIFO for Each Endpoint</li> </ul>
PHY Interface	* On-Chip UTMI PHY Parallel Interface
Maximum Operating Frequency	<ul style="list-style-type: none"> <li>* 12 External Oscillator (Main Oscillator)</li> <li>* 30MHz with 16bits parallel interface</li> </ul>

Table 2.10 nano PHY for USB2.0 OTG and USB1.1 Host

UTMI PHY	Key Features
Supported Specification	* Compliant with USB 2.0 Transceiver Macrocell Interface Spec. Ver-1.04
General Features	* 480Mbps High Speed / 12Mbps Full Speed, FS Only, 1.5Mbps Low Speed * Separate 8/16 bit Unidirectional Parallel Interface * Dual-Mode Device Support (HS/FS) * Data and Clock Recovery from Serial Data on the USB Connector * SYNC/End-Of-Packet Generation and Checking * Bit Stuffing and unstuffing, Bit-stuffing Error Detection * NRZI Encoding/Decoding * Support of Suspend, Resume, Remote Wakeup Operations * Integrated HS and FS Termination and Signaling Switching * On-Chip PLL for 480Mbps * Low Power Dissipation while Active, Idle, or on Standby
System Features	* 45-Ohm Termination / 1.5k Pull-up 15k Pull-down Integrated * Minimal External Components – Single Resistor
Maximum Operating Frequency	* up to 480MHz

Table 2.11 External Host Interface

EHI	Key Features
SRAM Type Interface	* 68/80 Series Interface with 8/16 Bit Width * Burst Transfer and Address Auto-Increment * Internal Interrupt Generation by an External Host Device * Semaphore Register for Improving Data Transfer Efficiency * READY can be Checked via Status Register and Pin. * LOCK MODE: External Host Device can Occupy System bus without any Handover.
Host Booting Procedure	* Configures 8/16 Bits Host Booting Mode * Host Downloads the Program into On-Chip SRAM or Off-Chip Memory * Restarts with Downloaded Program Code
Peak Access Bandwidth	* 8 Bits Configuration : 20MB/s * 16 Bits Configuration : 40MB/s

Table 2.12 SD/MMC Controller

SD/MMC	Key Features
Supported Specification	* SD ver.2.0 * SDIO ver.2.0 * MMC ver.4.3 * Ce-ATA Digital Protocol rev1.1
General Features	* Automatic CRC Generation & Checking the Data/Command * Data transmit/receive FIFO (32bits x 8) * Supported SD/MMC Mode → 1 Bit Serial or 4 Bit Parallel SD → 1 Bit Serial for MMC → 4/8 Bits Parallel Transfer * External DMA Handshaking for Burst & Fast Transfer
Maximum Frequency	* up to 50MHz <sup>1</sup> * Clock generation block Inside

Table 2.13 Memory Stick Controller

Memory Stick	Key Features
Supported Specifications	* Memory Stick Ver.1.x * Memory Stick Pro * Memory Stick Pro-HG
General Features	* Data transmit/receive FIFO (64bits x 4) * External DMA Handshaking for Burst & Fast Transfer
Maximum Operating Frequency	* Memory Stick serial clock (Serial : 20MHz, Parallel : 40MHz)

<sup>1</sup> The maximum operating frequency for storage devices can be limited by the system configuration and corresponding interface ports.

Table 2.14 Nand Flash Controller

NAND I/F	Key Features
NAND I/F	<ul style="list-style-type: none"> <li>* Automatic Detection of External READY Signal</li> <li>* Configurable Cycle Times based-on Bus Frequency</li> <li>* 8bit, 16bit, 32bit Interface to Buffer Memory</li> <li>* 8x32Bits FIFO Included</li> <li>* External DMA Handshaking for Burst and Fast Transfer</li> </ul>
External Configuration	<ul style="list-style-type: none"> <li>* 1 NAND - Single 8 bit NAND / Single 16bit NAND</li> <li>* 2 NAND - Double Series 8 bit NAND / Double Series 16 Bit NAND</li> <li>* 4 NAND - Double Parallel &amp; Series 8 Bit NAND</li> </ul>
SLC	<ul style="list-style-type: none"> <li>* 2 Bit Error Detection &amp; 1 Bit Error Correction per 256 bytes.</li> <li>* Configurable Memory Regions for ECC Calculations</li> </ul>
MLC	<ul style="list-style-type: none"> <li>* 4/8/12/14/16 Bit Error Detection/Correction Based on BCH Algorithm</li> <li>* 8x32 FIFO</li> </ul>

Table 2.15 IDE interface

HDD (UDMA)		Key Features			
Supported Specification	* It Supports for the following mode. - maximum theoretical bandwidths for various operating mode				
	PIO MODE	SPEED	UDMA MODE	SPEED	
	PIO MODE 0	3.3 MBps	MODE 0	16.67 MBps	
	PIO MODE 1	5.22 MBps	MODE 1	25 MBps	
	PIO MODE 2	8.33 MBps	MODE 2	33.33 MBps	
	PIO MODE 3	11.11 MBps	MODE 3	44.44 MBps	
	PIO MODE 4	16.67 MBps	MODE 4	66.67 MBps	
	General Features		* It has a 16x32 bit FIFO that supports internal DMA operation.		
Maximum Operating Frequency		TBD			

Table 2.16 UART Interface

UART	Key Features
General Features	<ul style="list-style-type: none"> <li>* 16 bytes TX/RX FIFO</li> <li>* Support of Hardware Flow Control ( CTS/RTS )</li> <li>* 16 bits clock divider</li> <li>* 16C550 Compatible Core</li> <li>* <b>Smart Card Interface</b></li> </ul>
Maximum Operating Frequency	* Baud Rate Clock ( 3MHz ← 48MHz / 16 )

Table 2.17 GPSB Interface

GPSB	Key Features
General Feature	<ul style="list-style-type: none"> <li>* MSB / LSB Selection mode</li> <li>* Support Variable transfer (1~16bit)</li> <li>* Clock frequency/ Polarity selection mode</li> <li>* Support configurable Frame signal mode</li> </ul>
Maximum Operating Frequency	<ul style="list-style-type: none"> <li>* 60MHz for slave only</li> <li>* 30MHz for master mode</li> </ul>

Table 2.18 General DMA Controller

General DMA	Key Features
General Features	<ul style="list-style-type: none"> <li>* 12-Channel DMA</li> <li>* Dedicated Bus Interface for Various Storage Interface Controllers</li> <li>* Support of Byte/Half-word/Word Transfer</li> <li>* Support of Circular Buffer Interface</li> <li>→ Masking of the Source/Destination Address Bits</li> <li>* 1/2/4/8 Burst Transfers</li> <li>* Byte Swapping Function</li> <li>* Support of Single/Continuous/Burst Mode</li> <li>* 8x32bits FIFO Included</li> </ul>
DMA Request/Acknowledge	<ul style="list-style-type: none"> <li>* External DMA Request/Acknowledge</li> <li>* Interfacing the On-chip Storage Controllers</li> </ul>
Inter-channel Arbitration	<ul style="list-style-type: none"> <li>* Configurable Priority for Each Channel</li> <li>* Round-robin Arbitration / Fixed Priority Arbitration</li> </ul>

Table 2.19 Vectored Interrupt Controller

VPIC	Key Features
General Features	<ul style="list-style-type: none"> <li>* 64 Individual Interrupt Sources</li> <li>* FIQ/IRQ Configurable</li> <li>* Priority Reconfigurable for Each Interrupt Sources</li> <li>* Polarity Controllable</li> <li>* Edge/Level Sensitivity Controllable</li> <li>* Dual/Single Edge Controllable when Edge Sensitivity Selected</li> </ul>
Vectored Interrupt Handler	<ul style="list-style-type: none"> <li>* Vector ID Returned for Fast Handling</li> <li>* Vector ID is one of 0 ~ 63</li> <li>* 64x32 Vector Table Needed for Vector Handler on On-Chip Memory</li> </ul>

Table 2.20 Timer

TIMER & WDT	Key Features
Timer Counters	<ul style="list-style-type: none"> <li>* Four 16-bit timers with PWM output/counters, two 20-bit timers, and one 32-bit timer</li> <li>* External Event Counter</li> <li>* Stop Mode / Free Running Mode</li> <li>* Various Clock Sources ( PLL outputs ~ Divided Sub-Clock )</li> <li>* PWM Functions → TREFn, TMREFn</li> </ul>
Watchdog Timers	<ul style="list-style-type: none"> <li>* Watchdog Timer Interrupt / Reset</li> </ul>

Table 2.21 ADC

TSADC	Key Features
General Features	* 12bit Resolution * 0 ~ 3.3V Input Range ( In case of 3.3V AVDD)
Operating Frequency	* 1MSPS / 5MHz
Touch Screen	* X/Y Position * Up/Down Wake-up

Table 2.22 Real Time Clock

RTC	Key Features
General Features	* Sub Oscillator Included * Clock and Calendar Function (BCD Display) → Sec/Min/Hour/Date/Day-of-Week/Month/Year * Leap Year Generation * Wakeup Signal Generation from the Deep Power-down Mode
Interrupt & Round Reset	* Alarm Interrupt in Normal Operation Mode * Cyclic interrupts 1/256, 1/64, 1/16, 1/4, 1/2, 1 second interrupts * Round-reset function 30-, 40-, 50- second
Wakeup Function	* Dedicated Wake-up Port

### 3 PIN Description

#### 3.1 TCC8900 Pin Description

**Table 3.1 Power/Ground Information**

Group	# of Balls	Ball#	MIN(V)	TYP(V)	MAX(V)	Description
GNDCORE	17	F4, J5, F7, L7, T9, E10, E12, U12, K13, M13, N13, R13, K14, J15, P15, R15, K16	-	-	-	Internal Core Ground
PWRCORE	15	H4, J4, F6, R8, G9, G11, G12, P13, W13, H14, J14, L15, N15, T15, M4	1.14	1.20	1.26	Digital Internal Core Power @ $F_{CPU} \leq 500\text{MHz}$
			TBD	TBD	TBD	@ $F_{CPU} \leq 600\text{MHz}$
GNDIO	9	P4, H5, F8, E11, T11, V11, F12, E14, F15	-	-	-	I/O Ground
PWRGPIOA	1	V13				GPIOA Group I/O Power
PWRGPIOB	2	F11, F9				GPIOB Group I/O Power
PWRGPIOC	2	E6, E9	1.71	1.8	1.89	GPIOC Group I/O Power
PWRGPIOD	2	F13, F14	2.38	2.5	2.62	GPIOD Group I/O Power
PWRGPIOE	2	V10, V12	3.14	3.3	3.46	GPIOE Group I/O Power
PWRGPIOF	2	G4, P5				GPIOF Group I/O Power
PWRETC	1	G14	1.8		3.6	ETC Group I/O Power
PWRMEMQ	6	J13, L14, M14, M15, N14, P14	1.71	1.8	1.89	SDR/DDR/mDDR I/O Power
PWRMEMZQ	1	J12	2.38	2.5	2.62	DDR2 ZQ Calibration Power
			3.14	3.3	3.46	
GNDMEMZQ	1	H12	-	-	-	SDR/DDR/mDDR/DDR2 I/F Ground
PWROSC	1	L6	2.7	3.0	3.3	Oscillator Power
GNDOSC	1	M6	-	-	-	Oscillator Ground
PWRUSB12	1	L4	1.14	1.20	1.26	UTMI Digital Core Power
PWRUSB33	1	L5	3.0	3.3	3.6	UTMI Analog Core Power
GNDUSB	1	K1	-	-	-	UTMI Ground
PWRUSBH	1	B11				USB 1.1 Host Transceiver Power
GNDUSBH	1	B10				USB 1.1 Host Transceiver Ground
PWRLVDS33A	2	P7, R7				LVDS Transmitter Power
GNDLVDS33A	3	T6, W5, Y5				LVDS Transmitter Ground
PWRSATA1	1	R4	1.14	1.20	1.26	SATA Core Power 1
PWRSATA2	1	P3	1.14	1.20	1.26	SATA Core Power 2
GNDATA	2	M1, R1				SATA Core Ground
PWRSATAOSC	1	U2	3.0	3.3	3.6	SATA Oscillator Power
GNDATAOSC	1	V1				SATA Oscillator Ground
PWRSATAPLL	1	P2	1.14	1.20	1.26	SATA PLL Power
GNDATAPLL	1	R2				SATA PLL Ground
PWRHDMI	1	T5	1.14	1.20	1.26	HDMI Core Power
GNDHDMI	3	V2, V3, U6				HDMI Core Ground
PWRHDMIPLL1	1	R5	1.14	1.20	1.26	HDMI PLL Power 1
PWRHDMIPLL2	1	T4	1.14	1.20	1.26	HDMI PLL Power 2
GNDHDMIPLL	1	R6				HDMI PLL Ground
PWRHDMIOSC	1	U5	3.0	3.3	3.6	HDMI Oscillator Power
GNDHDMIOSC	1	V5				HDMI Oscillator Ground
PWRADC	1	T13	2.7 <sup>1</sup>	3.3	3.6	ADC Power
GNDADC	1	T14	-	-	-	ADC Ground
PWRDAC	1	U9	2.7	3.0	3.3	DAC Power
GNDDAC	2	T8, U7	-	-	-	DAC Ground
PWRPLL	1	N5	1.14	1.20	1.26	PLL Power
GNDPLL	1	M3	-	-	-	PLL Ground
PWRRTC	1	N4	1.5	3.0	3.3	RTC Core & I/O Power

<sup>1</sup> PWRADC : When PWRADC is 2.7~3.0V, note that ADC error rate is increased.

Table 3.2 PWRGPIOC Group I/O Pin Description

NAME	BALL	I/O <sup>1</sup>	INIT <sup>2</sup>	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
GPIOC[0]	A9	B	IU	GPIOC[0]	LXD[0]	L0_LPD[0]	TSD5(3)		L1_LPD[0]	GPIOF[0]
GPIOC[1]	A8	B	IU	GPIOC[1]	LXD[1]	L0_LPD[1]	TSD6(3)		L1_LPD[1]	GPIOF[1]
GPIOC[2]	B9	B	IU	GPIOC[2]	LXD[2]	L0_LPD[2]	TSD7(3)		L1_LPD[2]	GPIOF[2]
GPIOC[3]	C9	B	IU	GPIOC[3]	LXD[3]	L0_LPD[3]			L1_LPD[3]	GPIOF[3]
GPIOC[4]	B8	B	IU	GPIOC[4]	LXD[4]	L0_LPD[4]			L1_LPD[4]	GPIOF[4]
GPIOC[5]	D9	B	IU	GPIOC[5]	LXD[5]	L0_LPD[5]			L1_LPD[5]	GPIOF[5]
GPIOC[6]	E8	B	IU	GPIOC[6]	LXD[6]	L0_LPD[6]	SDO(3)		L1_LPD[6]	GPIOF[6]
GPIOC[7]	A7	B	IU	GPIOC[7]	LXD[7]	L0_LPD[7]	SDI(3)		L1_LPD[7]	GPIOF[7]
GPIOC[8]	C8	B	I	GPIOC[8]	LXD[8]	L0_LPD[8]	SCLK(3)		L1_LPD[8]	GPIOF[8]
GPIOC[9]	D8	B	I	GPIOC[9]	LXD[9]	L0_LPD[9]	SFRM(3)		L1_LPD[9]	GPIOF[9]
GPIOC[10]	B7	B	I	GPIOC[10]	LXD[10]	L0_LPD[10]	SDO(2)		L1_LPD[10]	GPIOF[10]
GPIOC[11]	A6	B	I	GPIOC[11]	LXD[11]	L0_LPD[11]	SDI(2)		L1_LPD[11]	GPIOF[11]
GPIOC[12]	C7	B	I	GPIOC[12]	LXD[12]	L0_LPD[12]	SCLK(2)		L1_LPD[12]	GPIOF[12]
GPIOC[13]	D7	B	I	GPIOC[13]	LXD[13]	L0_LPD[13]	SFRM(2)		L1_LPD[13]	GPIOF[13]
GPIOC[14]	E7	B	I	GPIOC[14]	LXD[14]	L0_LPD[14]	SD_D7(0)	MS_D7(0)	L1_LPD[14]	GPIOF[14]
GPIOC[15]	C6	B	I	GPIOC[15]	LXD[15]	L0_LPD[15]	SD_D6(0)	MS_D6(0)	L1_LPD[15]	GPIOF[15]
GPIOC[16]	B6	B	I	GPIOC[16]	LXD[16]	L0_LPD[16]	SD_D5(0)	MS_D5(0)	L1_LPD[16]	GPIOF[16]
GPIOC[17]	A5	B	I	GPIOC[17]	LXD[17]	L0_LPD[17]	SD_D4(0)	MS_D4(0)	L1_LPD[17]	GPIOF[17]
GPIOC[18]	A4	B	IU	GPIOC[18]	LXD[18]	L0_LPD[18]	SD_D3(0)	MS_D3(0)	L1_LPD[18]	
GPIOC[19]	B5	B	IU	GPIOC[19]	LXD[19]	L0_LPD[19]	SD_D2(0)	MS_D2(0)	L1_LPD[19]	
GPIOC[20]	D6	B	IU	GPIOC[20]	LXD[20]	L0_LPD[20]	SD_D1(0)	MS_D1(0)	L1_LPD[20]	
GPIOC[21]	C5	B	IU	GPIOC[21]	LXD[21]	L0_LPD[21]	SD_D0(0)	MS_D0(0)	L1_LPD[21]	
GPIOC[22]	B4	B	I	GPIOC[22]	LXD[22]	L0_LPD[22]	SD_CLK(0)	MS_CLK(0)	L1_LPD[22]	
GPIOC[23]	A3	B	I	GPIOC[23]	LXD[23]	L0_LPD[23]	SD_CMD(0)	MS_BUS(0)	L1_LPD[23]	
GPIOC[24]	D5	B	IU	GPIOC[24]	LWEN	L0_LDE	TSD4(3)		L1_LDE	GPIOF[19]
GPIOC[25]	C4	B	IU	GPIOC[25]	LOEN	L0_LCK	TSD3(3)		L1_LCK	GPIOF[18]
GPIOC[26]	B3	B	I	GPIOC[26]	LXA[0]	L0_LHS	TSD2(3)		L1_LHS	GPIOF[22]
GPIOC[27]	E5	B	IU	GPIOC[27]	LCSN0	L0_LVS	TSD1(3)		L1_LVS	GPIOF[20]
GPIOC[28]	A2	B	IU	GPIOC[28]	LCSN1	SDO(10)	TSVALID(3)			GPIOF[21]
GPIOC[29]	C3	B	I	GPIOC[29]		SDI(10)	TSCLK(3)			
GPIOC[30]	D4	B	I	GPIOC[30]	EXTLVS0(0)	SCLK(10)	TSD0(3)			
GPIOC[31]	B2	B	I	GPIOC[31]	EXTLVS1(0)	SFRM(10)	TSSYNC(3)			

<sup>1</sup> I/O type. B = bi-direction, I = Input, O = Output

<sup>2</sup> INIT column represents the corresponding I/O state while the reset signal is asserted.

OL = output low, OH = output high, O = output unknown, IU = input/pull-up, ID = input /pull-down, I = input floating



Table 3.3 PWRGPIOF Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
BPEN	F5	B	I	BPEN	BPEN	BPEN	BPEN	BPEN	BPEN	BPEN
GPIOF[0]	A1	B	I	GPIOF[0]	HPXD[0]	SD_D0(3)	HDDXD0	TSD0(0)	MS_D0(3)	EDIXA[3]
GPIOF[1]	D3	B	I	GPIOF[1]	HPXD[1]	SD_D1(3)	HDDXD1	TSD1(0)	MS_D1(3)	EDIXA[4]
GPIOF[2]	B1	B	I	GPIOF[2]	HPXD[2]	SD_D2(3)	HDDXD2	TSD2(0)	MS_D2(3)	EDIXA[5]
GPIOF[3]	E4	B	I	GPIOF[3]	HPXD[3]	SD_D3(3)	HDDXD3	TSD3(0)	MS_D3(3)	EDIXA[6]
GPIOF[4]	C2	B	I	GPIOF[4]	HPXD[4]	SD_D4(3)	HDDXD4	TSD4(0)	MS_D4(3)	EDIXA[7]
GPIOF[5]	C1	B	I	GPIOF[5]	HPXD[5]	SD_D5(3)	HDDXD5	TSD5(0)	MS_D5(3)	EDIXA[8]
GPIOF[6]	D2	B	I	GPIOF[6]	HPXD[6]	SD_D6(3)	HDDXD6	TSD6(0)	MS_D6(3)	EDIXA[9]
GPIOF[7]	E3	B	I	GPIOF[7]	HPXD[7]	SD_D7(3)	HDDXD7	TSD7(0)	MS_D7(3)	EDIXA[10]
GPIOF[8]	E2	B	I	GPIOF[8]	HPXD[8]	SD_CMD(3)	HDDXD8	TSVALID(0)	MS_BUS(3)	EDIXA[11]
GPIOF[9]	F3	B	I	GPIOF[9]	HPXD[9]	SD_CLK(3)	HDDXD9	TSCLK(0)	MS_CLK(3)	EDIXA[12]
GPIOF[10]	F2	B	I	GPIOF[10]	HPXD[10]	SDO(7)	HDDXD10	TSSYNC(0)		EDIXA[13]
GPIOF[11]	D1	B	I	GPIOF[11]	HPXD[11]	SDI(7)	HDDXD11			EDIXA[14]
GPIOF[12]	E1	B	I	GPIOF[12]	HPXD[12]	SCLK(7)	HDDXD12			EDIXA[15]
GPIOF[13]	G3	B	I	GPIOF[13]	HPXD[13]	SFRM(7)	HDDXD13			EDIXA[16]
GPIOF[14]	F1	B	I	GPIOF[14]	HPXD[14]	SDO(8)	HDDXD14			EDIXA[17]
GPIOF[15]	G2	B	I	GPIOF[15]	HPXD[15]	SDI(8)	HDDXD15			EDIXA[18]
GPIOF[16]	G1	B	I	GPIOF[16]	HPXD[16]	SCLK(8)	HDDXA0			
GPIOF[17]	H2	B	I	GPIOF[17]	HPXD[17]	SFRM(8)	HDDXA1			
GPIOF[18]	H3	B	I	GPIOF[18]	HPRDN	SD_D3(1)	HDDXA2	MS_D3(1)		
GPIOF[19]	J2	B	I	GPIOF[19]	HPWRN	SD_D2(1)	HDDCSN1	MS_D2(1)		
GPIOF[20]	J3	B	I	GPIOF[20]	HPCSN0	SD_D1(1)	HDDRDY	MS_D1(1)		
GPIOF[21]	J6	B	I	GPIOF[21]	HPCSN1	SD_D0(1)	HDDCSN0	MS_D0(1)		
GPIOF[22]	K7	B	I	GPIOF[22]	HPXA	SD_CMD(1)	HDDAK	MS_BUS(1)		
GPIOF[23]	K2	B	I	GPIOF[23]	HPINT0	SD_CLK(1)	HDDRQ	MS_CLK(1)		
GPIOF[24]	K4	B	I	GPIOF[24]	HPINT1	SDO(9)	HDDIOW			
GPIOF[25]	K3	B	I	GPIOF[25]		SDI(9)	HDDIOR			
GPIOF[26]	K6	B	I	GPIOF[26]	EXTLVS1(1)	SCLK(9)	CAN_RX			
GPIOF[27]	K5	B	I	GPIOF[27]	EXTLVS0(1)	SFRM(9)	CAN_TX			

Table 3.4 PWRGPIOE Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
GPIOE[0]	N7	B	IU	GPIOE[0]	UTXD(0)					
GPIOE[1]	P8	B	IU	GPIOE[1]	URXD(0)					
GPIOE[2]	U10	B	IU	GPIOE[2]	UCTS(0)	SFRM(5)				
GPIOE[3]	M7	B	IU	GPIOE[3]	URTS(0)	SCLK(5)				
GPIOE[4]	L8	B	IU	GPIOE[4]	UTXD(1)					
GPIOE[5]	N8	B	IU	GPIOE[5]	URXD(1)					
GPIOE[6]	R9	B	IU	GPIOE[6]	UCTS(1)	SDI(5)	SD_CLK(4)	MS_CLK(4)		
GPIOE[7]	U11	B	IU	GPIOE[7]	URTS(1)	SDO(5)	SD_CMD(4)	MS_BUS(4)		
GPIOE[8]	W11	B	I	GPIOE[8]	UTXD(2)	SFRM(4)	SD_D0(4)	MS_D0(4)		
GPIOE[9]	Y11	B	I	GPIOE[9]	URXD(2)	SCLK(4)	SD_D1(4)	MS_D1(4)		
GPIOE[10]	Y12	B	I	GPIOE[10]	UTXD(3)	SDI(4)	SD_D2(4)	MS_D2(4)		
GPIOE[11]	T10	B	I	GPIOE[11]	URXD(3)	SDO(4)	SD_D3(4)	MS_D3(4)		
GPIOE[12]	Y13	B	I	GPIOE[12]	CPD[0]	SD_D0(2)	TSD0(1)	MS_D0(2)		
GPIOE[13]	P9	B	I	GPIOE[13]	CPD[1]	SD_D1(2)	TSD1(1)	MS_D1(2)		
GPIOE[14]	Y14	B	I	GPIOE[14]	CPD[2]	SD_D2(2)	TSD2(1)	MS_D2(2)		
GPIOE[15]	M8	B	I	GPIOE[15]	CPD[3]	SD_D3(2)	TSD3(1)	MS_D3(2)		
GPIOE[16]	Y15	B	IU	GPIOE[16]	CPD[4]	SD_D4(2)	TSD4(1)	MS_D4(2)		
GPIOE[17]	L9	B	IU	GPIOE[17]	CPD[5]	SD_D5(2)	TSD5(1)	MS_D5(2)		
GPIOE[18]	W12	B	IU	GPIOE[18]	CPD[6]	SD_D6(2)	TSD6(1)	MS_D6(2)		
GPIOE[19]	R10	B	IU	GPIOE[19]	CPD[7]	SD_D7(2)	TSD7(1)	MS_D7(2)		
GPIOE[20]	Y16	B	IU	GPIOE[20]	CCKI	SD_CLK(2)	TSCLK(1)	MS_CLK(2)		
GPIOE[21]	P10	B	IU	GPIOE[21]	CVS	SD_CMD(2)	TSSYNC(1)	MS_BUS(2)		
GPIOE[22]	Y17	B	IU	GPIOE[22]	CHS		TSVALID(1)			
GPIOE[23]	R11	B	IU	GPIOE[23]	CCKO	CFIELD				

Table 3.5 PWRGPIOA Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
GPIOA[0]	Y18	B	IU	GPIOA[0]	SCL0					
GPIOA[1]	T12	B	IU	GPIOA[1]	SDA0					
GPIOA[2]	W14	B	I	GPIOA[2]	CLK_OUT0					
GPIOA[3]	N9	B	I	GPIOA[3]	CLK_OUT1					
GPIOA[4]	W15	B	IU	GPIOA[4]	WDTRSTO	TCO0				
GPIOA[5]	M9	B	IU	GPIOA[5]	IRDI	TCO1				
GPIOA[6]	W16	B	IU	GPIOA[6]	HDMI_CECO	TCO2				EDIXA[19]
GPIOA[7]	N10	B	IU	GPIOA[7]	HDMI_CECI	TCO3				EDIXA[20]
GPIOA[8]	V15	B	IU	GPIOA[8]	SCL1					
GPIOA[9]	M10	B	IU	GPIOA[9]	SDA1					
GPIOA[10]	U14	B	I	GPIOA[10]	CBCLK(0)	CBCLK(1)				
GPIOA[11]	U13	B	I	GPIOA[11]	CLRCK(0)	CLRCK(1)				
GPIOA[12]	V14	B	I	GPIOA[12]	CDATA(0)	CDATA(1)				
GPIOA[13]	P11	B	I	GPIOA[13]	EXTCLKI					
GPIOA[14]	N11	B	I	GPIOA[14]	HDMI_HPD	TCO4				
GPIOA[15]	R12	B	I	GPIOA[15]	UTM_DRVVBUS	TCO5				

Table 3.6 PWRADC Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
AIN[0]	V16	B	I	GPIOE[24]	AIN[0]					
AIN[1]	U15	B	I	GPIOE[25]	AIN[1]					
AIN[2]	W17	B	I	GPIOE[26]	AIN[2]	SD_CMD(7)	MS_BUS(7)			
AIN[3]	W18	B	I	GPIOE[27]	AIN[3]	SD_CLK(7)	MS_CLK(7)			
AIN[4]	Y19	B	I	GPIOE[28]	TSC_YM	SD_D0(7)	MS_D0(7)			
AIN[5]	V17	B	I	GPIOE[29]	TSC_YP	SD_D1(7)	MS_D1(7)			
AIN[6]	U16	B	I	GPIOE[30]	TSC_XM	SD_D2(7)	MS_D2(7)			
AIN[7]	R14	B	I	GPIOE[31]	TSC_XP	SD_D3(7)	MS_D3(7)			

Table 3.7 PWRETC Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
BM[0]	H16	I	I	BM[0]						
BM[1]	G15	I	I	BM[1]						
BM[2]	C20	I	I	BM[2]						
TDO	B20	O	O	TDO						
TEST	B19	I	I	TEST						
RSTN	C19	I	I	RSTN						
NTRST	E17	I	I	NTRST						
TMS	D17	I	I	TMS						
TCK	F16	I	I	TCK						
TDI	E16	I	I	TDI						
RTCK	E15	O	O	RTCK						

Table 3.8 PWRGPIOD Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
GPIOD[0]	A20	B	IU	GPIOD[0]	BCLK(1)	BCLK(0)				
GPIOD[1]	D16	B	IU	GPIOD[1]	LRCK(1)	LRCK(0)				
GPIOD[2]	A19	B	IU	GPIOD[2]	MCLK(1)	MCLK(0)				
GPIOD[3]	C17	B	IU	GPIOD[3]	DAO0(1)	DAO0(0)				
GPIOD[4]	C18	B	IU	GPIOD[4]	DAI0(1)	DAI0(0)				
GPIOD[5]	A18	B	IU	GPIOD[5]	DAO1(1)	SFRM(11)				
GPIOD[6]	B18	B	IU	GPIOD[6]	DAI1(1)	SCLK(11)				
GPIOD[7]	A17	B	IU	GPIOD[7]	DAO2(1)	SDI(11)				
GPIOD[8]	G13	B	I	GPIOD[8]	DAI2(1)	SDO(11)				
GPIOD[9]	D15	B	I	GPIOD[9]	DAO3(1)	SFRM(6)	TSD7(2)			
GPIOD[10]	H13	B	I	GPIOD[10]	DAI3(1)	SCLK(6)	TSD6(2)			
GPIOD[11]	C16	B	I	GPIOD[11]	SPD_TX(1)	SDI(6)	SPD_TX(0)			
GPIOD[12]	L11	B	I	GPIOD[12]	SPD_RX(1)	SDO(6)	TSSYNC(2)			
GPIOD[13]	B17	B	I	GPIOD[13]	UTXD(4)		TSD5(2)			
GPIOD[14]	L10	B	I	GPIOD[14]	URXD(4)		TSD4(2)			
GPIOD[15]	C15	B	I	GPIOD[15]	UCTS(4)	SFRM(12)	TSVALID(2)			
GPIOD[16]	K11	B	IU	GPIOD[16]	URTS(4)	SCLK(12)	TSCLK(2)			
GPIOD[17]	D14	B	IU	GPIOD[17]	UTXD(5)		TSD3(2)			
GPIOD[18]	J11	B	IU	GPIOD[18]	URXD(5)		TSD2(2)			
GPIOD[19]	B16	B	IU	GPIOD[19]	UCTS(5)	SDI(12)	TSD1(2)			
GPIOD[20]	K10	B	IU	GPIOD[20]	URTS(5)	SDO(12)	TSD0(2)			
GPIOD[21]	A16	B	IU	GPIOD[21]						
GPIOD[22]	K8	B	IU	GPIOD[22]						
GPIOD[23]	C14	B	IU	GPIOD[23]						
GPIOD[24]	K9	B	I	GPIOD[24]						
GPIOD[25]	D13	B	I	GPIOD[25]						

Table 3.9 PWRGPIOB Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
GPIOB[0]	J7	B	IU	GPIOB[0]	EDIXD8	SD_D0(5)	MS_D0(5)			
GPIOB[1]	B15	B	IU	GPIOB[1]	EDIXD9	SD_D1(5)	MS_D1(5)			
GPIOB[2]	J10	B	IU	GPIOB[2]	EDIXD10	SD_D2(5)	MS_D2(5)			
GPIOB[3]	E13	B	IU	GPIOB[3]	EDIXD11	SD_D3(5)	MS_D3(5)			
GPIOB[4]	J8	B	IU	GPIOB[4]	EDIXD4	SD_D4(5)	MS_D4(5)			
GPIOB[5]	B14	B	IU	GPIOB[5]	EDIXD5	SD_D5(5)	MS_D5(5)			
GPIOB[6]	J9	B	IU	GPIOB[6]	EDIXD6	SD_D6(5)	MS_D6(5)			
GPIOB[7]	C13	B	IU	GPIOB[7]	EDIXD7	SD_D7(5)	MS_D7(5)			
GPIOB[8]	H11	B	I	GPIOB[8]	EDIXD0			SFRM(1)		
GPIOB[9]	A15	B	I	GPIOB[9]	EDIXD1			SCLK(1)		
GPIOB[10]	H10	B	I	GPIOB[10]	EDIXD2			SDI(1)		
GPIOB[11]	D12	B	I	GPIOB[11]	EDIXD3			SDO(1)		
GPIOB[12]	H6	B	I	GPIOB[12]	EDIXD12	SD_CMD(5)	MS_BUS(5)			
GPIOB[13]	B13	B	I	GPIOB[13]	EDIXD13	SD_CLK(5)	MS_CLK(5)			
GPIOB[14]	F10	B	I	GPIOB[14]	EDIXD14					
GPIOB[15]	A14	B	I	GPIOB[15]	EDIXD15					
GPIOB[16]	G10	B	I	GPIOB[16]	EDIWEN0					
GPIOB[17]	A13	B	I	GPIOB[17]	EDIWEN1 <sup>1</sup>			SFRM(0)		
GPIOB[18]	H7	B	I	GPIOB[18]	EDIOEN0					
GPIOB[19]	A12	B	I	GPIOB[19]	EDIOEN1 <sup>2</sup>			SCLK(0)		
GPIOB[20]	H9	B	I	GPIOB[20]	EDIXA[0] <sup>3</sup>					
GPIOB[21]	D11	B	I	GPIOB[21]	EDIXA[1] <sup>4</sup>	SD_D4(6)	MS_D4(6)			
GPIOB[22]	H8	B	IU	GPIOB[22]	EDIXA[2]	SD_D5(6)	MS_D5(6)			
GPIOB[23]	C12	B	IU	GPIOB[23]	EDICSN0 <sup>5</sup>	SD_D6(6)	MS_D6(6)			
GPIOB[24]	G5	B	IU	GPIOB[24]	EDICSN1	SD_D7(6)	MS_D7(6)			
GPIOB[25]	B12	B	IU	GPIOB[25]	EDICSN2	SD_D0(6)	MS_D0(6)			
GPIOB[26]	G6	B	IU	GPIOB[26]	EDICSN3	SD_D1(6)	MS_D1(6)			
GPIOB[27]	C11	B	IU	GPIOB[27]	EDICSN4	SD_D2(6)	MS_D2(6)			EDIXA[23]
GPIOB[28]	G7	B	I	GPIOB[28]	EDIRDY0 <sup>6</sup>	SD_D3(6)	MS_D3(6)			
GPIOB[29]	D10	B	I	GPIOB[29]	EDIRDY1	SD_CMD(6)	MS_BUS(6)			
GPIOB[30]	G8	B	IU	GPIOB[30]	EDICSN5	SD_CLK(6)	MS_CLK(6)	SDI(0)		EDIXA[22]
GPIOB[31]	C10	B	IU	GPIOB[31] <sup>6</sup>	EDICSN6			SDO(0)		EDIXA[21]

<sup>1</sup> Dedicated to NAND WEN signal for NAND booting

<sup>2</sup> Dedicated to NAND OEN signal for NAND booting

<sup>3</sup> Dedicated to NAND CLE signal for NAND booting

<sup>4</sup> Dedicated to NAND ALE signal for NAND booting

<sup>5</sup> Dedicated to NAND CSN0 signal for NAND booting

<sup>6</sup> Dedicated to NAND Ready signal for NAND booting. Either EDIRDY0 or GPIOB[31] can be used for NAND ready signal as described in the BOOT PROCEDURE in datasheet.

Table 3.10 PWRMEMQ Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0 (DDR2-2CS)	FUNC1 (DDR2-1CS)	FUNC2 (DDR/mDDR)	FUNC3 (SDR)	FUNC4	FUNC5	FUNC6
DRAM XD28	W19			XD28	XD28	XD28	XD28			
DRAM XD27	U17			XD27	XD27	XD27	XD27			
DRAM XD25	T17			XD25	XD25	XD25	XD25			
DRAM XD30	Y20			XD30	XD30	XD30	XD30			
DRAM DQM3	V18			DQM3	DQM3	DQM3	DQM3			
DRAM DQS3	U18			DQS3	DQS3	DQS3				
DRAM DQSB3	T18			DQSB3	DQSB3	-				
DRAM XD31	U19			XD31	XD31	XD31	XD31			
DRAM XD24	V19			XD24	XD24	XD24	XD24			
DRAM XD26	W20			XD26	XD26	XD26	XD26			
DRAM XD29	V20			XD29	XD29	XD29	XD29			
DRAM XD20	R16			XD20	XD20	XD20	XD20			
DRAM XD19	T19			XD19	XD19	XD19	XD19			
DRAM XD17	U20			XD17	XD17	XD17	XD17			
DRAM XD22	T20			XD22	XD22	XD22	XD22			
DRAM DQM2	R17			DQM2	DQM2	DQM2	DQM2			
DRAM DQS2	R18			DQS2	DQS2	DQS2				
DRAM DQSB2	P18			DQSB2	DQSB2	-				
DRAM XD23	R19			XD23	XD23	XD23	XD23			
DRAM XD16	R20			XD16	XD16	XD16	XD16			
DRAM XD18	P17			XD18	XD18	XD18	XD18			
DRAM XD21	P19			XD21	XD21	XD21	XD21			
DRAM CLKB	P20			CLKB	CLKB	CLKB	-			
DRAM CLK	N20			CLK	CLK	CLK	CLK			
DRAM XA6	M20			XA6	XA6	XA6	XA6			
DRAM XA12	P12			XA12	XA12	XA12	XA12			
DRAM XA11	N19			XA11	XA11	XA11	XA11			
DRAM RASN	N18			RASN	RASN	RASN	RASN			
DRAM XA0	N12			XA0	XA0	XA0	XA0			
DRAM XA5	N17			XA5	XA5	XA5	XA5			
DRAM XA10	N16			XA10	XA10	XA10	XA10			
DRAM CASN	M11			CASN	CASN	CASN	CASN			
DRAM CSN1	M17			CSN1	XA13	CSN1	CSN1			
DRAM XA2	M18			XA2	XA2	XA2	XA2			
DRAM ODT0	M12			ODT0	ODT0		XA14			
DRAM CSN0	M19			CSN0	CSN0	CSN0	CSN0			
DRAM BA0	L19			BA0	BA0	BA0	BA0			
DRAM BA2	L18			BA2	BA2	XA13	XA13			
DRAM XA3	M16			XA3	XA3	XA3	XA3			
DRAM BA1	L17			BA1	BA1	BA1	BA1			
DRAM XA1	L13			XA1	XA1	XA1	XA1			
DRAM XA4	L16			XA4	XA4	XA4	XA4			
DRAM XA7	K19			XA7	XA7	XA7	XA7			
DRAM ODT1	L12			ODT1	XA14	CKE1	CKE1			
DRAM XA9	J20			XA9	XA9	XA9	XA9			
DRAM CKE	K18			CKE	CKE	CKE0	CKE0			
DRAM XA8	K12			XA8	XA8	XA8	XA8			
DRAM WEN	K17			WEN	WEN	WEN	WEN			
DRAM XD12	H20			XD12	XD12	XD12	XD12			
DRAM XD11	G20			XD11	XD11	XD11	XD11			
DRAM XD9	F20			XD9	XD9	XD9	XD9			
DRAM XD14	H19			XD14	XD14	XD14	XD14			
DRAM DQM1	J19			DQM1	DQM1	DQM1	DQM1			
DRAM DQS1	J18			DQS1	DQS1	DQS1				
DRAM DQSB1	J17			DQSB1	DQSB1	-				
DRAM XD15	G19			XD15	XD15	XD15	XD15			
DRAM XD8	J16			XD8	XD8	XD8	XD8			
DRAM XD10	H17			XD10	XD10	XD10	XD10			
DRAM XD13	H18			XD13	XD13	XD13	XD13			
DRAM XD4	E20			XD4	XD4	XD4	XD4			
DRAM XD3	F19			XD3	XD3	XD3	XD3			
DRAM XD1	D20			XD1	XD1	XD1	XD1			
DRAM XD6	E19			XD6	XD6	XD6	XD6			
DRAM DQM0	F18			DQM0	DQM0	DQM0	DQM0			
DRAM DQS0	G18			DQS0	DQS0	DQS0				
DRAM DQSB0	G17			DQSB0	DQSB0	-				
DRAM XD7	D19			XD7	XD7	XD7	XD7			
DRAM XD0	D18			XD0	XD0	XD0	XD0			
DRAM XD2	E18			XD2	XD2	XD2	XD2			
DRAM XD5	F17			XD5	XD5	XD5	XD5			
DRAM VREF0	H15			VREF0	VREF0					
DRAM VREF1	K15			VREF1	VREF1					
DRAM VREF2	P16			VREF2	VREF2					
DRAM VREF3	T16			VREF3	VREF3					
DRAM GATEI	L20			GATEI	GATEI	GATEI				
DRAM GATEO	K20			GATEO	GATEO	GATEO				
DRAM ZQ	G16			ZQ	ZQ	ZQ				

Table 3.11 PWROSC Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
XI	L2	I		XI						
XO	L1	O		XO						

Table 3.12 PWRUSB33 Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
OTG_VBUS	L3			OTG_VBUS						
OTG_DP	H1			OTG_DP						
OTG_DM	J1			OTG_DM						
OTG_REXT	M2			OTG_REXT						

Table 3.13 PWRUSBH Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
UBH_DP	A11			UBH_DP						
UBH_DM	A10			UBH_DM						

Table 3.14 PWRRTC Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0						
RTC_XTI	N3	I		RTC_XTI						
RTC_XTO	N2	O		RTC_XTO						
RTC_PMWKUP	M5	O	OH	RTC_PMWKUP						
RTC_RSTN	N6	I	IL	RTC_RSTN						

Table 3.15 PWRSATAOSC Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0						
SATA_XI	R3	I		SATA_XI						
SATA_XO	T3	O		SATA_XO						

Table 3.16 PWRSATA Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0						
SATA_REXT	T2			SATA_REXT						
SATA_TXP	U1			SATA_TXP						
SATA_TXN	T1			SATA_TXN						
SATA_RXP	N1			SATA_RXP						
SATA_RXN	P1			SATA_RXN						

Table 3.17 PWRHDMIOSC Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0						
HDMI_XI	U4			HDMI_XI						
HDMI_XO	U3			HDMI_XO						

Table 3.18 PWRHDMI Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0						
HDMI_TXCP	Y1			HDMI_TXCP						
HDMI_TXCN	W1			HDMI_TXCN						
HDMI_TX0P	Y2			HDMI_TX0P						
HDMI_TX0N	W2			HDMI_TX0N						
HDMI_TX1P	Y3			HDMI_TX1P						
HDMI_TX1N	W3			HDMI_TX1N						
HDMI_TX2P	Y4			HDMI_TX2P						
HDMI_TX2N	W4			HDMI_TX2N						
HDMI_REXT	V4			HDMI_REXT						

Table 3.19 PWRLVDS Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0						
LVDS_TCLKP	V6			LVDS_TCLKP						
LVDS_TCLKN	V7			LVDS_TCLKN						
LVDS_TEP	Y6			LVDS_TEP						
LVDS_TEN	W6			LVDS_TEN						
LVDS_ROUT	P6			LVDS_ROUT						
LVDS_TDP	Y7			LVDS_TDP						
LVDS_TDN	W7			LVDS_TDN						
LVDS_TCP	Y8			LVDS_TCP						
LVDS_TCN	W8			LVDS_TCN						
LVDS_TBP	Y9			LVDS_TBP						
LVDS_TBN	W9			LVDS_TBN						
LVDS_TAP	Y10			LVDS_TAP						
LVDS_TAN	W10			LVDS_TAN						

Table 3.20 PWRDAC Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0						
DAC_OUT	U8			DAC_OUT						
DAC_COMP	T7			DAC_COMP						
DAC_IREF	V8			DAC_IREF						
DAC_VREF	V9			DAC_VREF						



## 3.2 TCC8900 I/O Type

Table 3.21 TCC8900 I/O Type

TYPE	Diagram	DESCRIPTION	PAD Name
A		cmos input with controllable pull-up/down and output PAD	TDO RTCK PMWKUP
B		analog and digital mixed PAD	AIN[0]~AIN[7]
C		cmos input, bypass input and output PAD	GPIOF Group
D		cmos input with controllable pull-up/down, output, and bypass output PAD	GPIOC Group
E		schmitt trigger input with controllable pull-up/down and output PAD	GPIOA Group GPIOB Group GPIOD Group GPIOE Group
F		schmitt trigger input	BPEN RSTN BM[2]~BM[0] TEST
G		Real Time Clock Oscillator	XTIN,XTOUT

H		oscillator for XIN/XOUT	XIN,XOUT
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## 4 Package Information

### 4.1 Dimension

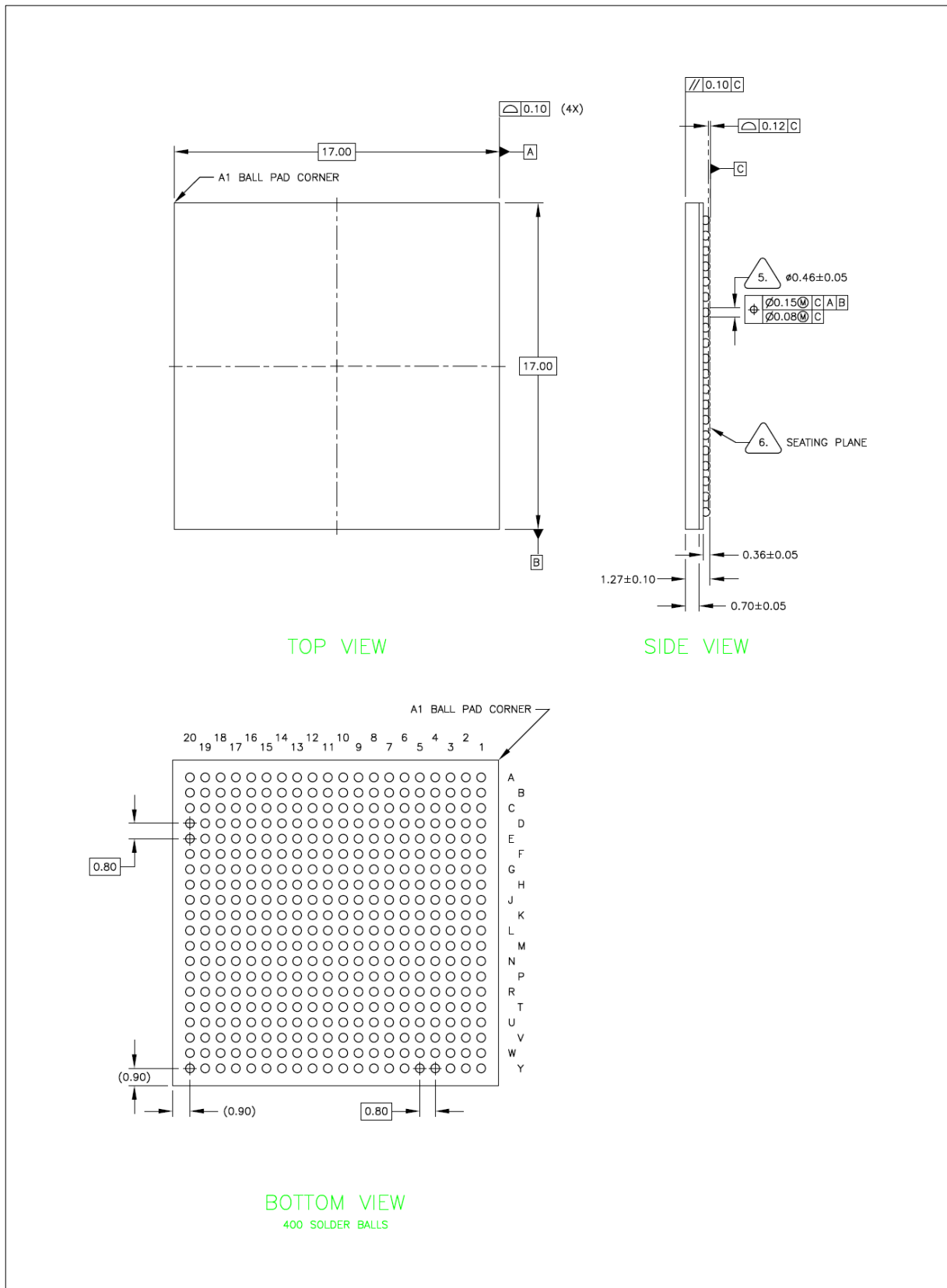


Figure 4.1 TCC8900 Package Dimension

## 4.2 Ball Map

S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	BGA1
A	GPIO[0]	GPIO[28]	GPIO[23]	GPIO[18]	GPIO[17]	GPIO[11]	GPIO[7]	GPIO[1]	GPIO[0]	UBH_DM	UBH_DP	GPIO[19]	GPIO[17]	GPIO[15]	GPIO[8]	GPIO[21]	GPIO[7]	GPIO[5]	GPIO[2]	GPIO[0]	A
B	GPIO[2]	GPIO[31]	GPIO[26]	GPIO[21]	GPIO[19]	GPIO[16]	GPIO[10]	GPIO[4]	GPIO[2]	GPIO[2]	PWRUSSH	GPIO[25]	GPIO[13]	GPIO[5]	GPIO[1]	GPIO[19]	GPIO[13]	GPIO[6]	TEST	TDO	B
C	GPIO[5]	GPIO[4]	GPIO[29]	GPIO[25]	GPIO[21]	GPIO[15]	GPIO[12]	GPIO[8]	GPIO[3]	GPIO[3]	GPIO[27]	GPIO[23]	GPIO[7]	GPIO[23]	GPIO[15]	GPIO[11]	GPIO[3]	GPIO[4]	RSTN	BM[2]	C
D	GPIO[11]	GPIO[6]	GPIO[1]	GPIO[30]	GPIO[24]	GPIO[20]	GPIO[13]	GPIO[9]	GPIO[5]	GPIO[29]	GPIO[21]	GPIO[11]	GPIO[25]	GPIO[17]	GPIO[9]	GPIO[1]	TMS	DRAM_X00	DRAM_X07	DRAM_X01	D
E	GPIO[12]	GPIO[8]	GPIO[7]	GPIO[3]	GPIO[27]	PWRPROC	GPIO[14]	GPIO[6]	PWRPROC	GPIO[29]	GPIO[21]	GPIO[11]	GPIO[25]	GPIO[17]	GPIO[9]	GPIO[1]	NTST	DRAM_X02	DRAM_X06	DRAM_X04	E
F	GPIO[14]	GPIO[10]	GPIO[9]	GPIO[3]	BREN	PWRCORE	GPIO[14]	GPIO[6]	PWRPROC	GPIO[29]	GPIO[21]	GPIO[11]	GPIO[25]	GPIO[17]	GPIO[9]	GPIO[1]	TDI	DRAM_X02	DRAM_X06	DRAM_X04	F
G	GPIO[16]	GPIO[15]	GPIO[13]	PWRPROC	GPIO[24]	GPIO[26]	GPIO[28]	GPIO[30]	PWRCORE	GPIO[16]	PWRCORE	PWRCORE	GPIO[8]	PWRETC	BM[1]	DRAM_ZQ	DRAM_DCS0	DRAM_X05	DRAM_X03	DRAM_X09	G
H	OTG_DP	GPIO[17]	GPIO[18]	PWRCORE	GPIO[17]	GPIO[12]	GPIO[18]	GPIO[22]	GPIO[20]	GPIO[10]	GPIO[8]	GPIO[8]	GPIO[10]	PWRCORE	DRAM_VREF0	BM[0]	DRAM_XD10	DRAM_XD13	DRAM_XD14	DRAM_XD12	H
J	OTG_DM	GPIO[19]	GPIO[20]	PWRCORE	GPIO[19]	GPIO[21]	GPIO[8]	GPIO[4]	GPIO[6]	GPIO[2]	GPIO[18]	PWRCORE	PWRCORE	PWRCORE	GPIO[2]	DRAM_X08	DRAM_DCS1	DRAM_XD11	DRAM_XD15	DRAM_XD11	J
K	GNUSB	GPIO[23]	GPIO[25]	PWRCORE	GPIO[24]	GPIO[26]	GPIO[22]	GPIO[24]	GPIO[24]	GPIO[20]	GPIO[16]	DRAM_XA8	GNDCORE	GNDCORE	DRAM_VREF1	GNDCORE	DRAM_WEN	DRAM_OKE	DRAM_XA7	DRAM_GATE0	K
L	XO	XI	OTG_VBUS	PWRCORE	PWRCORE	PWRCORE	GPIO[22]	GPIO[22]	GPIO[24]	GPIO[24]	GPIO[12]	DRAM_C0T1	DRAM_XA1	PWRCORE	PWRCORE	DRAM_XA4	DRAM_BA1	DRAM_BA2	DRAM_BA0	DRAM_GATE1	L
M	GNDSATA	OTG_REXT	GNDFLL	PWRCORE	RTC_PWMAUP	GNOSC	GPIO[3]	GPIO[15]	GPIO[5]	GPIO[9]	DRAM_CASN	DRAM_C0T0	GNDCORE	GNDCORE	PWRCORE	DRAM_XA3	DRAM_CSN1	DRAM_XA2	DRAM_CSN0	DRAM_XA6	M
N	SATA_RXP	RTC_XTO	RTC_XTI	PWRCORE	PWRCORE	RTC_RSTN	GPIO[0]	GPIO[5]	GPIO[3]	GPIO[7]	GPIO[14]	DRAM_XA0	GNDCORE	GNDCORE	PWRCORE	DRAM_XA10	DRAM_XA5	DRAM_RASN	DRAM_XA11	DRAM_CLK	N
P	SATA_RXN	PWRSATA1LL	PWRSATA2	GNDCORE	PWRCORE	LVDS_ROUT	PWRLVDS33A	GPIO[1]	GPIO[3]	GPIO[21]	GPIO[13]	DRAM_XA12	PWRCORE	PWRCORE	GNDCORE	DRAM_VREF2	DRAM_XD18	DRAM_DCS2	DRAM_XD21	DRAM_CLKB	P
R	GNDSATA	GNDSATA1LL	SATA_XI	PWRSATA1	PWRCORE	GNDCORE	PWRLVDS33A	PWRCORE	GPIO[8]	GPIO[9]	GPIO[23]	GPIO[15]	GNDCORE	GNDCORE	GNDCORE	DRAM_XD20	DRAM_DCS2	DRAM_DCS2	DRAM_XD23	DRAM_XD16	R
T	SATA_TXN	SATA_REXT	SATA_XO	PWRCORE	PWRCORE	GNDCORE	DAC_COMP	GNDCORE	GPIO[11]	GPIO[11]	GPIO[27]	GPIO[11]	PWRCORE	GNDCORE	PWRCORE	DRAM_VREF3	DRAM_XD25	DRAM_DCS3	DRAM_XD19	DRAM_XD22	T
U	SATA_TXP	PWRSATAOSC	HDMI_XO	HDMI_XI	PWRCORE	GNDCORE	GNDCORE	DAC_OUT	PWRCORE	GPIO[2]	GPIO[27]	GNDCORE	GPIO[11]	GPIO[10]	GNDCORE	GNDCORE	DRAM_XD27	DRAM_DCS3	DRAM_XD31	DRAM_XD17	U
V	GNDSATAOSC	GNDCORE	GNDCORE	HDMI_REXT	GNDCORE	LVDS_TQXP	LVDS_TQKN	DAC_REF	DAC_VREF	PWRCORE	GNDCORE	PWRCORE	PWRCORE	GPIO[12]	GPIO[8]	GNDCORE	GNDCORE	DRAM_DCS3	DRAM_XD24	DRAM_XD23	V
W	HDMI_TXCN	HDMI_TXCN	HDMI_TXIN	HDMI_TX2N	GNDCORE	LVDS_TEN	LVDS_TDN	LVDS_TCN	LVDS_TBN	LVDS_TAN	GPIO[8]	GPIO[8]	PWRCORE	GPIO[2]	GPIO[4]	GPIO[6]	GNDCORE	GNDCORE	DRAM_XD28	DRAM_XD26	W
Y	HDMI_TXCP	HDMI_TXCP	HDMI_TXIP	HDMI_TX2P	GNDCORE	LVDS_TEN	LVDS_TDN	LVDS_TCN	LVDS_TBN	LVDS_TAN	GPIO[8]	GPIO[8]	PWRCORE	GPIO[2]	GPIO[4]	GPIO[6]	GNDCORE	GNDCORE	DRAM_XD28	DRAM_XD26	Y
BGA1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	BGA1

Figure 4.2 TCC8900 Ball Map

## 5 Electrical Specification

### 5.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
DC Supply Voltage for I/O (Various I/O power excepts for analog – ADC, DAC, PLL, USB)	$V_{DDIO}$	4.6	V
DC Supply Voltage for Internal Digital Logic (PWR12)	$V_{DDI}$	1.8	V
DC Supply Voltage for Analog Part of ADC (PWRADC)	$V_{DDADC}$	4.6	V
DC Supply Voltage for PLL (PWRPLL)	$V_{DDPLL}$	1.8	V
DC Supply Voltage for USB2.0 (PWRUSB)	$V_{DDUSB}$	4.6	V
DC Supply Voltage for RTC (PWRRTC)	$V_{DDRTC}$	4.6	V
Digital Input Voltage for Input Buffer	$V_{IN}$	4.6	V
Digital Output Voltage for Output Buffer	$V_{OUT}$	4.6	V
In/Out Current for Digital I/O	$I_{I/O}$	$\pm 20$	mA
Analog Input Voltage for ADC	$V_{IN\_ADC}$	$0 \sim V_{DDADC}$	V
Storage Temperature	$T_{STG}$	-55 to 150	°C

**Note:**

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and functional operation under any of these conditions is not implied.

- (1) All voltages are measured with respect to VSS unless otherwise specified.
- (2)  $V_{DDI}$  must always be less than  $V_{DDIO}$
- (3) The voltage difference between analog and digital grounds must always be within 0.3V.

## 5.2 Recommended Operating Conditions

Table 5.1 Recommended Operating Conditions<sup>1</sup>

Parameter	Symbol	MIN	TYP	MAX	Unit
Output Load Resistance for DAC [ $\pm 1\%$ tolerance]	$R_{LOAD}$	-	37.5	-	$\Omega$
Core (PWRCORE) and PLL (PWRPLL) supply Voltage @ $F_{CPU} \leq 500\text{MHz}$	$V_{DDI}$ $V_{DDPLL}$	1.14	1.2	1.26	V
Core (PWRCORE) and PLL (PWRPLL) supply Voltage @ $F_{CPU} \leq 600\text{MHz}$		TBD	TBD	TBD	
Operating Temperature [Extended]	$T_{OPER}$	-30		85	$^{\circ}\text{C}$
Operating Temperature [Industrial]	$T_{OPER}$	-40	-	85	$^{\circ}\text{C}$

<sup>1</sup> The recommended operating conditions for power/ground are described on the Power/Ground Information in the Pin Descriptions.

## 5.3 Recommended Operating Frequency

Table 5.2 Recommended Operating Frequency

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
XIN Oscillator	@ 1.2V(TYP)	F <sub>XIN</sub>	12	12	12	MHz
XTIN Oscillator	@ 1.2V(TYP)	F <sub>XTIN</sub>	32.768		32.768*128	KHz
Input Clock of Bus Clock Generator (1 ~ 7) <sup>23</sup>	@ 1.2V(TYP)	F <sub>BCLKGEN</sub>			910	MHz
Input Clock of CPU Clock Generator <sup>24</sup>	@ 1.2V(TYP)	F <sub>CPUGEN</sub>			500	MHz
Input Clock of PLL Divider	@ 1.2V(TYP)	F <sub>PLLDIVIN</sub>			830	MHz
Input Clock of I/O Clock Generator <sup>25</sup>	@ 1.2V(TYP)	F <sub>IOCLKGEN</sub>			500	MHz
ARM1176JZF-S Core Clock	@ 1.2V(TYP)	F <sub>CPU</sub>			500	MHz
Bus Clock of DDI Bus	@ 1.2V(TYP)	F <sub>BUS_DDI</sub>			240	MHz
Bus Clock of Graphic Bus	@ 1.2V(TYP)	F <sub>BUS_GRP</sub>			190	MHz
Bus Clock of I/O Bus	@ 1.2V(TYP)	F <sub>BUS_IOB</sub>			166	MHz
Bus Clock of SMU Controller	@ 1.2V(TYP)	F <sub>BUS_SMU</sub>			125	MHz
Bus Clock of Video Bus	@ 1.2V(TYP)	F <sub>BUS_VBUS</sub>			215	MHz
Core Clock of Video Codec	@ 1.2V(TYP)	F <sub>BUS_VCODEC</sub>			160	MHz
Bus Clock of Memory Interface	@ 1.2V(TYP)	F <sub>BUS_MEM</sub>			260	MHz
Operating Clock of Camera Interface <sup>4</sup>	@ 1.2V(TYP)	F <sub>IO_CIF</sub>			200	MHz
Operating Clock of EHI <sup>4</sup>	@ 1.2V(TYP)	F <sub>IO_EHI</sub>			166	MHz
Operating Clock of GPSB Controller <sup>26</sup>	@ 1.2V(TYP)	F <sub>IO_GPSB</sub>			166	MHz
Operating Clock of Memory Stick Controller <sup>4</sup>	@ 1.2V(TYP)	F <sub>IO_MSTICK</sub>			100	MHz
Operating Clock of SD/MMC Controller <sup>4</sup>	@ 1.2V(TYP)	F <sub>IO_SDMMC</sub>			100	MHz
Operating Clock of UART Controller <sup>4</sup>	@ 1.2V(TYP)	F <sub>IO_UART</sub>			166	MHz
Operating Clock of LCD Controller <sup>4</sup>	@ 1.2V(TYP)	F <sub>IO_LCD</sub>			166	MHz
Operating Clock of PMU	@ 1.2V(TYP)	F <sub>IO_PMU</sub>	12	12	12	MHz
Operating Clock of Timer	@ 1.2V(TYP)	F <sub>IO_TIMER</sub>			125	MHz
Operating Clock of TSIF(Not GPSB)	@ 1.2V(TYP)	F <sub>IO_TSIF</sub>			80	MHz
Operating Clock of SPDIF Transmitter/Receiver <sup>4</sup>	@ 1.2V(TYP)	F <sub>IO_SPDIF</sub>			100	MHz
Operating Clock of Audio (ADMA/DAI/CDIF) <sup>4</sup>	@ 1.2V(TYP)	F <sub>IO_AUDIO</sub>			166	MHz
Operating Clock of CAN <sup>4</sup>	@ 1.2V(TYP)	F <sub>IO_CAN</sub>			50	MHz
Operating Clock of I2C <sup>4</sup>	@ 1.2V(TYP)	F <sub>IO_I2C</sub>			16	MHz
Operating Clock of USB 1.1 Host	@ 1.2V(TYP)	F <sub>IO_USBH</sub>	48	48	48	MHz

→The maximum operating frequency can be changed without any notice until approved for mass production.

<sup>23</sup> The related clocks are F<sub>BUS\_DDI</sub>, F<sub>BUS\_GRP</sub>, F<sub>BUS\_MEM</sub>, F<sub>BUS\_VBUS</sub>, F<sub>BUS\_VCODEC</sub>, F<sub>BUS\_SMU</sub>, F<sub>BUS\_IOB</sub>.

<sup>24</sup> The related clock is F<sub>CPU</sub>.

<sup>25</sup> The prefix of related clocks is F<sub>IO\_</sub>.

<sup>26</sup> The operating frequencies of external interface are not same as this. More detailed information is described on the timing characteristics of I/O interface. Refer to the corresponding timing information.

## 5.4 Electrical Characteristics for Power Supply

Table 5.3 Peak Power Consumption

Parameter	Power	Condition	MIN	TYP	MAX	Unit
Internal Core Power	PWRCORE	@ 1.2V			TBD	mA
GPIO Power	PWRGPION, (n=A,B,C,D,E,F) PWRETC	@ 1.8V				
		@ 2.7V				
		@ 3.3V			TBD	mA
Memory I/O Power	PWRMEMQ, PWRMEMZQ	@ 1.8V				
		@ 2.5V				
		@ 3.3V			TBD	mA
Oscillator Power (XI/XO)	PWROSC	@ 3.3V			TBD	mA
USB 1.2 Power of nanoPHY	PWRUSB12	@ 1.2V			TBD	mA
USB 3.3 Power of nanoPHY	PWRUSB33	@ 3.3V			TBD	mA
USB 1.1 Host Tranceiver Power	PWRUSBH	@ 3.3V			TBD	mA
RTC Power	PWRRTC	@ 2.7V			TBD	mA

- The rests of the power which are not described in the above table are shown in the corresponding sub-section.
- **The value in the above table does not mean the average power.** Refer to this at the designing of the power circuit.



## 5.5 Electrical Characteristics for General I/O

Table 5.4 DC Electrical Specification for General I/O

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
High Level Input Voltage	$V_{IH}$		$0.7V_{DDIO}$		$V_{DDIO}+0.3$	V
Low Level Input Voltage	$V_{IL}$		-0.3		$0.3V_{DDIO}$	V
Hysteresis Voltage	$\Delta V$		$0.1V_{DDIO}$			V
High Level Input Current	$I_{IH}$	VIN = VDDIO, pull-down disabled	-10		10	$\mu A$
		VIN = VDDIO, pull-down enabled	TBD		TBD	$\mu A$
Low Level Input Current	$I_{IL}$	VIN = VSSIO, pull-up disabled	-10		10	$\mu A$
		VIN = VSSIO, pull-up enabled	TBD		TBD	$\mu A$
High Level Output Voltage	$V_{OH}$	IOH = -100 $\mu A$	$V_{DDIO}-0.2$			V
Low Level Output Voltage	$V_{OL}$	IOL = 100 $\mu A$			0.2	V
Tri-state Output Leakage Current	$I_{OZ}$	VOUT = VSSIO or VDDIO	-10		10	$\mu A$
Input capacitance	$C_{IN}$	Any input and Bidirectional buffers			5	pF
Output capacitance	$C_{OUT}$	Any output buffer			5	pF
XI/XO Frequency	$F_{OSC1}$		-	12	-	MHz
XTIN/XTOUT Frequency	$F_{OSC2}$	Normal High Drive = Normal * 128	-	32.768 4194.304	-	kHz

Ta = 25°C, VSS = 0.0V unless otherwise specified.

Note:

- (1) 12MHz is recommended for XI/XO frequency.
- (2) PLL Output Frequencies are determined by XI/XO frequency.

## 5.6 Electrical Characteristics for PLL

Table 5.5 DC Electrical Characteristics for PLL0

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Power Down Current	$I_{PD}$	$V_{DDPLL} = 1.2V$			80	$\mu A$
Power Consumption	$P_{DD}$	$V_{DDPLL} = 1.2V$			3.0	mW

Ta = 25oC unless otherwise specified.

Table 5.6 AC Electrical Characteristics for PLL0

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Input Frequency	$F_{in}$	$V_{DDPLL} = 1.2V$		12		MHz
VCO output frequency	$F_{vco}$	$V_{DDPLL} = 1.2V$	800	-	1600	MHz
Output Frequency	$F_{out}$	$V_{DDPLL} = 1.2V$	40		1600	MHz
Locking Time	$T_{LT}$	$V_{DDPLL} = 1.2V$			300	us

Ta = 25oC unless otherwise specified.

Table 5.7 DC Electrical Characteristics for PLL1/2/3

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Power Down Current	$I_{PD}$	$V_{DDPLL} = 1.2V$			80	$\mu A$
Power Consumption	$P_{DD}$	$V_{DDPLL} = 1.2V$			1.5	mW

Ta = 25oC unless otherwise specified.

Table 5.8 AC Electrical Characteristics for PLL1/2/3

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Input Frequency	$F_{in}$	$V_{DDPLL} = 1.2V$		12		MHz
VCO output frequency	$F_{vco}$	$V_{DDPLL} = 1.2V$	250	-	600	MHz
Output Frequency	$F_{out}$	$V_{DDPLL} = 1.2V$	8		600	MHz
Locking Time	$T_{LT}$	$V_{DDPLL} = 1.2V$			300	us

Ta = 25oC unless otherwise specified.

## 5.7 Electrical Characteristics for Video DAC

Table 5.9 DC Electrical Characteristics for DAC

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Resolution	Bit		-	-	10	bits
Conversion Rate	$F_{CLK}$		-	-	27	MHz
Differential Non-Linearity	DNL		-	-	$\pm 1$	LSB
Integral Non-Linearity	INL		-	-	$\pm 2.5$	LSB
Full Scale Output Voltage	$V_O$		1.17	1.3	1.43	V
Output Load	$R_{LOAD}$	$\pm 1\%$ tolerance		37.5		$\Omega$
External Reference Voltage	$V_{REF}$		-	1.26	-	V

(VDDDAC = 3.0V, VSSDAC = 0V, Power Down = OFF,  $T_{op} = 30^\circ \text{C}$ ,  
 $R(I_{REF}) = 1.2k\Omega$ , Load Resistance =  $37.5\Omega$  unless otherwise specified.)

## 5.8 Electrical Characteristics for ADC(for Touch Screen)

**Table 5.10 DC Electrical Characteristics for ADC**

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Resolution	Bit		-	-	10(TBD)	bits
Differential Non-Linearity	DNL	VREF=3.3V, GND=0V	-	-	±1(TBD)	LSB
Integral Non-Linearity	INL	VREF=3.3V, GND=0V	-	-	±3(TBD)	LSB
Offset Voltage	TOPOFF BOTOFF	VREF=3.3V, GND=0V	-	-	10(TBD)	LSB

(Converter Specifications: VDDADC= 3.3V, VSSADC= 0V, Top=25°C, VREF=3.3V, GND=0.0V unless otherwise specified)

**Table 5.11 AC Electrical Characteristics for ADC**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum conversion rate	fc	f <sub>CKIN</sub> = 5MHz	–	–	1	MSPS
Standby supply current	–	STBY = VDD	–	–	60(TBD)	uA
Dynamic supply current	IVDD	f <sub>CKIN</sub> = 5MHz (without system load)	–	3.0(TBD)	5(TBD)	mA
Reference current	IREF	VREF = 3.3V	–	0.4(TBD)	0.6(TBD)	mA
Total harmonic distortion	THD	f <sub>CKIN</sub> = 5MHz AINT = 50kHz	–	– 60(TBD)	– 56(TBD)	dB
Signal-to-noise & distortion ratio	SNDR	f <sub>CKIN</sub> = 5MHz AINT = 50kHz	48(TBD)	54(TBD)	–	dB

(Converter Specifications: VDDADC =3.3V, VSSADC=0V, Top=25°C, VREF=3.3V, GND=0.0V unless otherwise specified)  
VDDIO = 3.3V±0.3V

## 5.9 Electrical Characteristics for HDMI PHY

Table 5.12 DC Electrical Characteristics for HDMI PHY

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Normal Mode Operating Power	P <sub>CC</sub>	Internal Video PLL ON Internal Video PLL OFF	-	72 42	-	mW
Power-Down Mode Power	P <sub>PD</sub>	-	-	TBD	-	mW

Table 5.13 AC Electrical Characteristics for HDMI Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
HDMI Oscillator Frequency	F <sub>R</sub>	-	-	27		MHz
Frequency Tolerance	F <sub>TOL</sub>		-100		100	ppm
Duty Cycle	D <sub>C</sub>		40		60	%
Jitter	J <sub>CLKI</sub>	Peak-to-Peak Jitter RMS Jitter			100 7	ps ps

## 5.10 Electrical Characteristics for LVDS

Table 5.14 DC Electrical Characteristics for LVDS

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Output differential voltage	$V_{OD}$		3.0	3.3	3.6	V
Change in $V_{OD}$ between complementary output states	$DV_{OD}$	-	-		50	mV
Output offset voltage	$V_{OS}$		1.125	1.25	1.375	V
Change in $V_{OS}$ between complementary output states	$DV_{OS}$				50	mV
Dynamic Current	$I_{DD}$				70	mA
Power Down Current	$I_{PD}$				100	uA

Typical values measured at PWRLVDS=3.3V and TA=25 oC

Table 5.15 AC Electrical Characteristics for LVDS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TXCLKIN Period	$T_{TCP}$		10		40	ns
DLL Lock Time	$T_{DLL}$	-			100	us
Skew Between Channels	$T_{SK}$		-200		200	ps
Duty Cycle	$D_C$		40		60	%
Jitter	$J_{CLKI}$	Peak-to-Peak Jitter			100	ps
		RMS Jitter			7	ps

These values are measured at the typical condition.

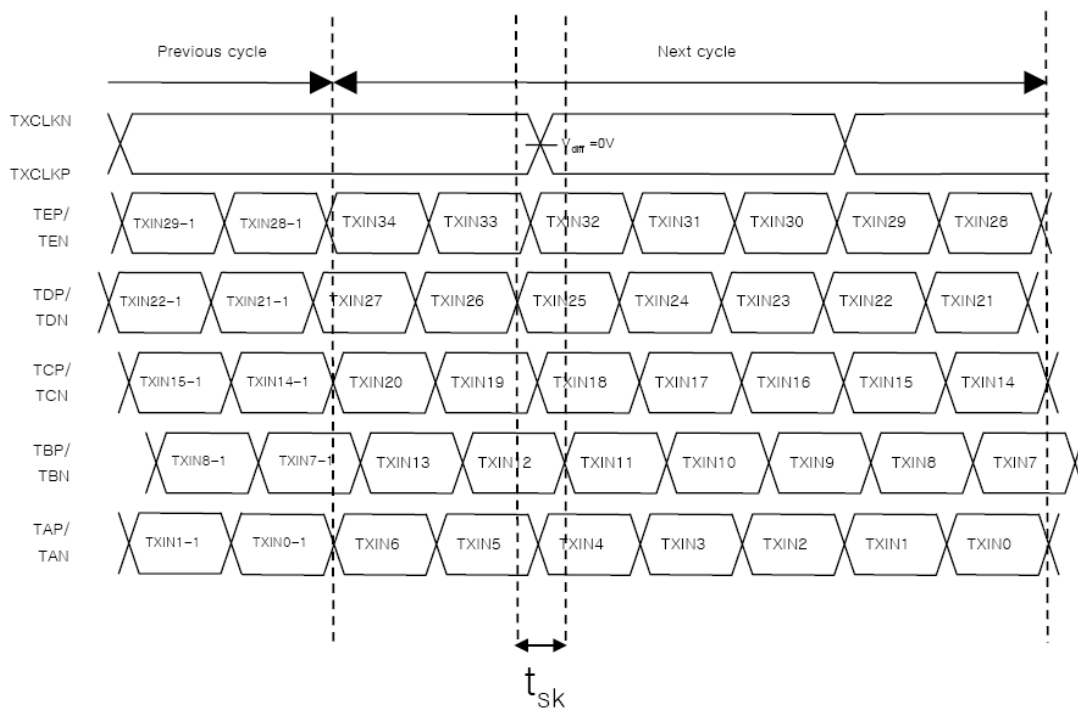


Figure 5.1 LVDS Transmit Timing Diagram

## 5.11 Electrical Characteristics for SATA

Table 5.16 DC Electrical Characteristics for SATA

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
TX serial data output voltage	DV <sub>TX</sub>	1.5Gbps 3.0Gbps	400 400		700 700	mVp-p
RX serial data input voltage	DV <sub>RX</sub>	1.5Gbps 3.0Gbps	325 275		600 750	mVp-p
Dynamic Current	I <sub>DD</sub>	Normal Mode Partial Mode		80 40		mW
Power Down Current	I <sub>PD</sub>	Slumber Mode		12		mW

All values in the above table are measured at typical condition.

Table 5.17 AC Electrical Characteristics for SATA Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillator Frequency	F <sub>R</sub>		–	25 100		MHz
Frequency Tolerance	F <sub>TOL</sub>		-100		100	ppm
Duty Cycle	D <sub>C</sub>		40		60	%
Clock Transition Time	T <sub>CLKT</sub>	Rising Falling			1.5 1.5	ns
Jitter	J <sub>CLKI</sub>	Peak-to-Peak Jitter RMS Jitter			40 2.5	ps ps

Table 5.18 AC Electrical Characteristics for SATA TX/RX

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Unit Interval	UI	1.5Gbps 3.0Gbps	–	666.67 333.33		ps
TX Serial Output Rise Time (20% → 80%)	T <sub>TX,RISE</sub>	1.5Gbps 3.0Gbps	100 67		273 136	ps
TX Serial Output Fall Time (80% → 20%)	D <sub>C</sub>	1.5Gbps 3.0Gbps	100 67		273 136	ps
TX Serial Data Output Voltage (Differential Peak-to-Peak)	D <sub>VTX</sub>	1.5Gbps 3.0Gbps	400 400		700 700	mVp-p
RX Serial Data Input Voltage (Differential Peak-to-Peak)	T <sub>RJ</sub>	1.5Gbps 3.0Gbps	325 275		600 750	mVp-p

## 5.12 Electrical Characteristics for LCD Interface

The following figure shows the timing diagram for TFT-LCD with RGB interface. All the timing parameters can be configured by LHTIME1, LHTIME2, LVTIME1 ~ 4 registers.

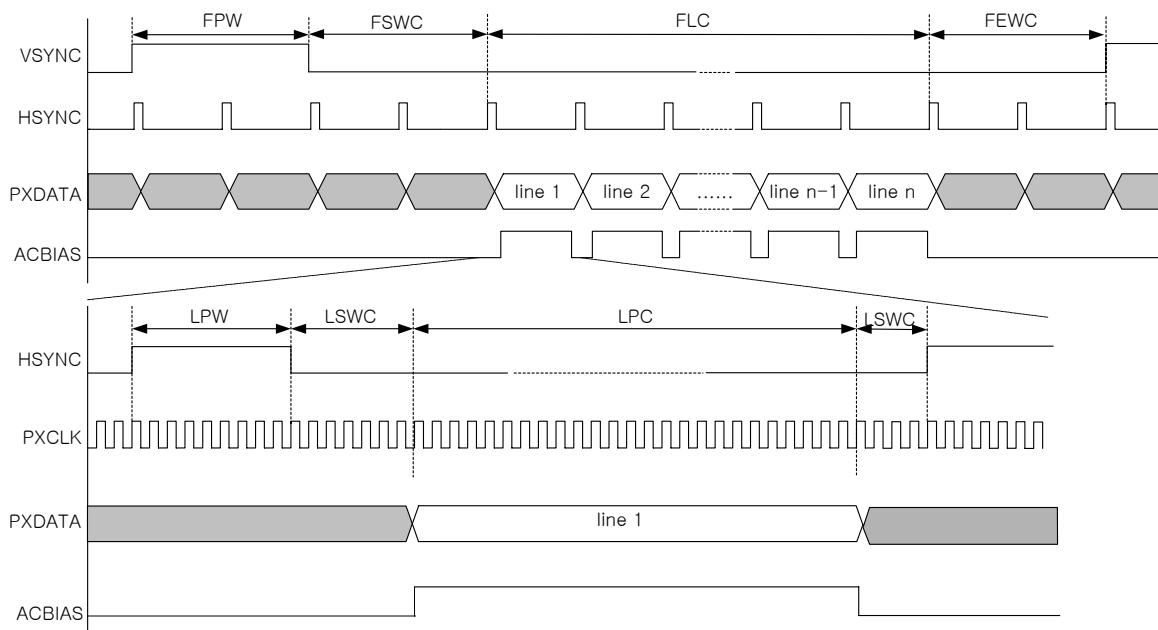


Figure 5.2 Timing Diagram for LCD Controller

The LHS (HSYNC), LVS (VSYNC), LBIAS (ACBIAS, Data Enable) and LPD[17:0] (PXDATA[17:0]) signals are referenced by LCK (PXCLK). Each min and max timing for the output delay are shown in the following figure.

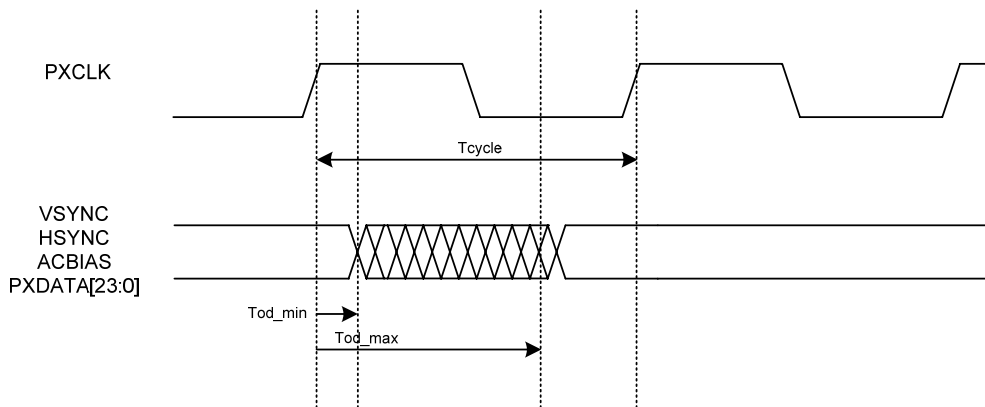


Figure 5.3 Timing Diagram Data Output Referenced to PXCLK

Table 5.19 Timing Parameters for Each Symbol

Parameter	Symbol	Min	Max	Unit	Remark
Clock Cycle	$T_{CYCLE}$	10	-	ns	
Output Delay	$T_{OD}$	0	7	ns	

Table 5.20 I/O Function Name for Corresponding Signal Name

Signal Name	I/O Function Name
VSYNC	L0_LVS, L1_LVS
HSYNC	L0_LHS, L1_LHS
ACBIAS	L0_LDE, L1_LDE
PXDATA[23:0]	L0_LPD[23:0], L1_LPD[23:0]
PXCLK	L0_LCK, L1_LCK

The following figure shows the timing diagram of bus interface to CPU I/F LCD device. The reference clock is used internally and the cycle time is defined as the register value written by software.



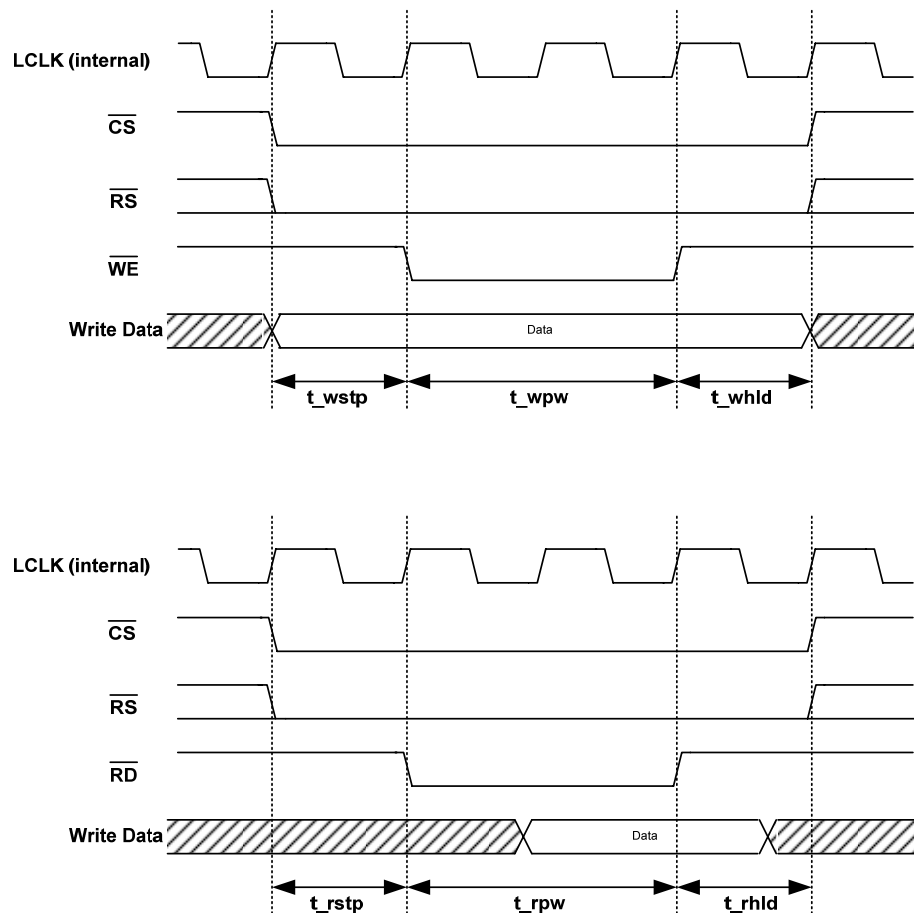


Figure 5.4 Timing Diagram Data Output Referenced to LCDSI

Table 5.21 Timing Parameters for Each Symbols

Parameter	Symbol	Min	Max	Unit	Remark
LCLK Clock Period (LCDSI Clock)	tCLK	18		ns	
RD/WE Setup Time Referenced to LCLK	T_rstp	0 * tCLK	7 * tCLK	ns	
RD/WE Pulse Width Referenced to LCLK	T_rpw	1 * tCLK	256 * tCLK	ns	
RD/WE Hold Time Referenced to LCLK	T_rhld	0 * tCLK	7 * tCLK	ns	

Signal Name	I/O Function Name
#CS	LCSN0, LCSN1
#RS	LXA[0]
#RD	LOEN
#WE	LWEN
Write Data[17:0]	LXD[17:0]

### 5.13 Electrical Characteristics for Camera Interface

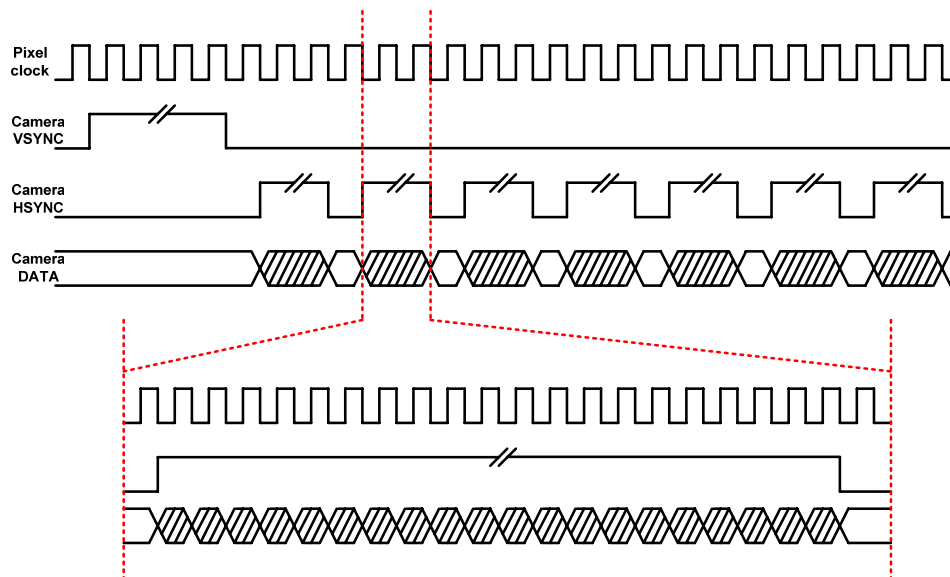


Figure 5.5 Timing Diagram for Camera Interface

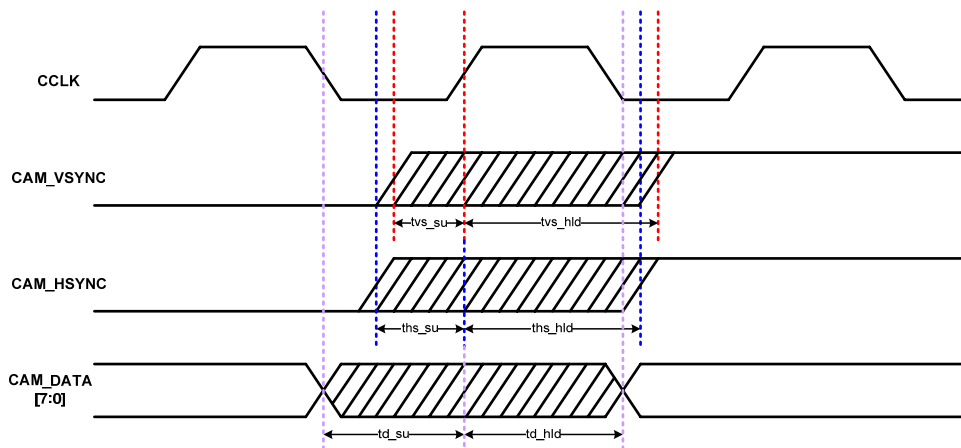


Figure 5.6 Timing Diagram Data Output Referenced to CCLK

Table 5.22 Timing Parameters for Each Symbol

Parameter	Symbol	Min	Max	Unit	Remark
Clock Frequency	TCLK		120	MHz	
Setup time for CVS(CAM_VSYNC)	Tvs_su	2		ns	
Hold time for CVS(CAM_VSYNC)	Tvs_hld	2		ns	
Setup time for CHS(CAM_HSYNC)	Ths_su	2		ns	
Hold time for CHS(CAM_HSYNC)	Ths_hld	2		ns	
Setup time for CPD[7:0](CAM_DATA)	Td_su	2		ns	
Hold time for CPD[7:0](CAM_DATA)	Td_hld	2		ns	

Table 5.23 I/O Function Name for Corresponding Signal Name

Signal Name	I/O Function Name
CCLK	CCKI
CAM_VSYNC	CVS
CAM_HSYNC	CHS
CAM_DATA[7:0]	CPD[7:0]

## 5.14 Electrical Characteristics for External Host Interface (EHI)

The EHI has two clock inputs; one is HCLK, which is for the on-chip system bus, the other is ECLK, which is for interface with the external host device. Therefore, interface timing with the external host is only related with ECLK.

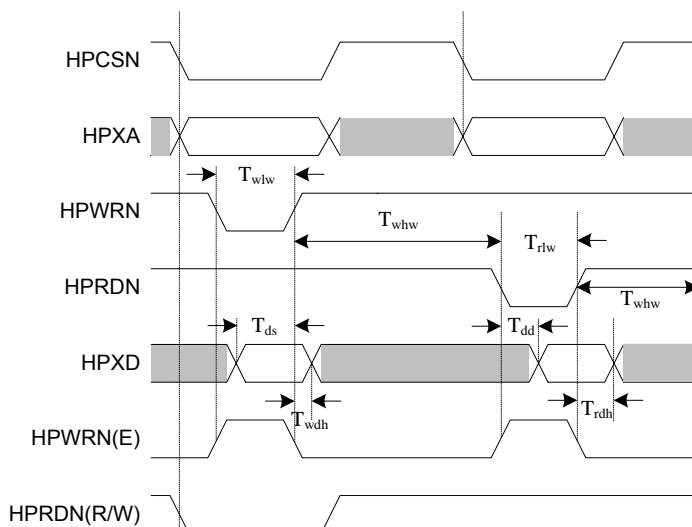


Figure 5.7 EHI Timing Diagram

Symbol	Description	Min.	Max.	Unit
$T_{w\text{lw}}$	Write low width	$2TP^{27}$	-	ns
$T_{w\text{hw}}$	Write high width	3TP	-	ns
$T_{r\text{lw}}$	Read low width	4TP	-	ns
$T_{r\text{hw}}$	Read high width	3TP	-	ns
$T_{\text{ds}}$	Data setup time	10	-	ns
$T_{\text{wdh}}$	Write data hold	5	25ns	ns
$T_{\text{dd}}$	Data delay time	-	$3TP + 10\text{ns}$	-
$T_{\text{rdh}}$	Read data hold	0	-	ns

<sup>27</sup> TP = ECLK period (ns)

### 5.15 Electrical Characteristics for SD/MMC Controller

The SD/MMC host controller is designed to supports high-speed mode (SD rev.1.10, up to 50 MHz Clock) as well as default speed mode (SD rev.1.01, up to 25 MHz Clock). A user doesn't need to set differently our SD/MMC host controller for mode change between default mode and high speed mode. If you want to change mode to high-speed mode from default mode and vice versa, by using switch-function command (CMD6), the SD/MMC cards are set to such mode. The timing diagram shows the input/output timing criterion referenced to SD/MMC clock.

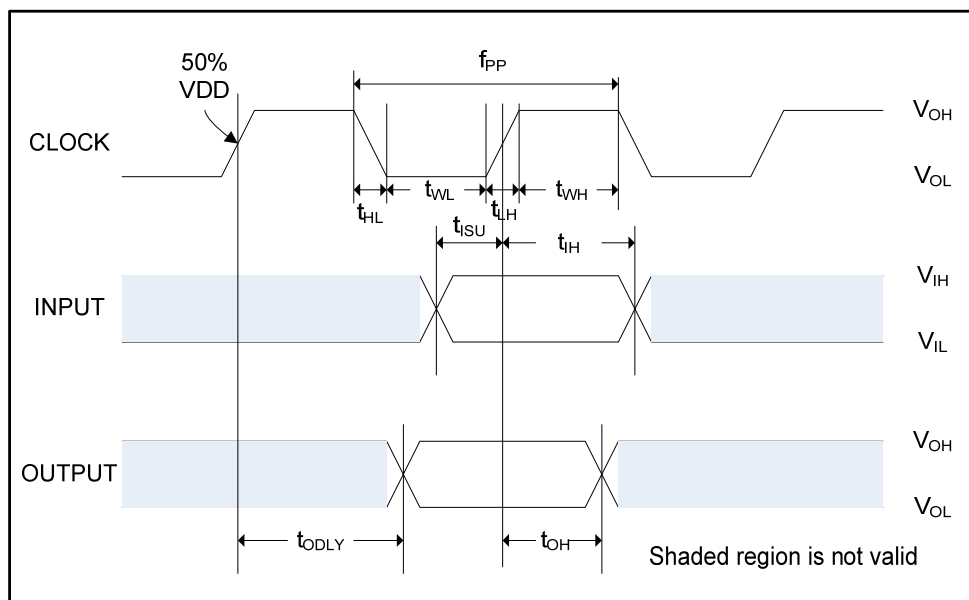


Figure 5.8 Timing Diagram for SD/MMC Controller

Table 5.24 Timing Parameters for Each Symbol

Parameter	Symbol	Min	Max	Unit	Remark
Clock frequency Data Transfer Mode	$f_{PP}$	0	50	MHz	$C_{card} \leq 30pF$
Clock low time	$t_{WL}$	7		ns	$C_{card} \leq 30pF$
Clock high time	$t_{WH}$	7		ns	$C_{card} \leq 30pF$
Clock rise time	$t_{LH}$		3	ns	$C_{card} \leq 30pF$
Clock fall time	$t_{HL}$		3	ns	$C_{card} \leq 30pF$
Input set-up time	$t_{ISU}$	6		ns	$C_{card} \leq 30pF$
Input hold time	$t_{IH}$	2.5		ns	$C_{card} \leq 30pF$
Output delay time	$t_{ODLY}$	10		ns	$C_{card} \leq 30pF$
Output hold time	$t_{OH}$	2		ns	$C_{card} \leq 30pF$

## 5.16 Electrical Characteristics for I2C Controller

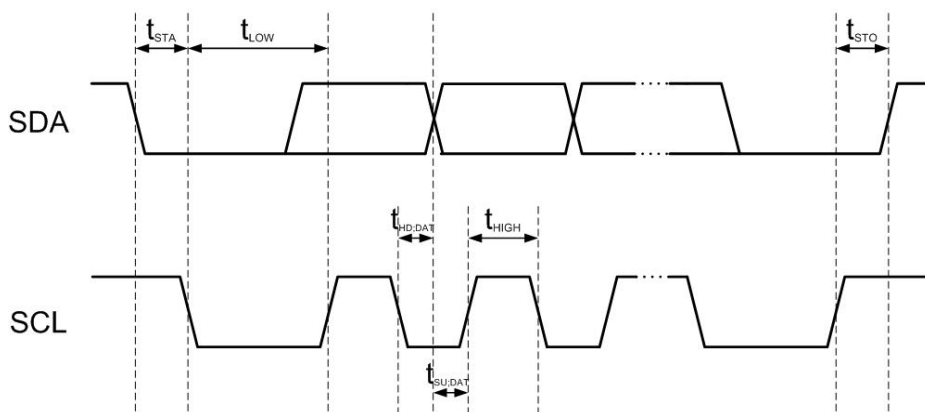


Figure 5.9 Timing Diagram for I2C Controller

Table 5.25 Timing Parameters for Each Symbol

Parameter	Symbol	Min	Max	Unit	Remark
SCL clock frequency		0	400	KHz	
Hold time(repeated) START condition	tSTA	0.95	-	us	
Data hold time	tHD:DAT	0.9		us	
Data setup time	tSU:DAT	0.4	-	us	
HIGH period of the SCL clock	tHIGH	0.96	-	us	
LOW period of the SCL clock	tLOW	1.4	-	us	
Setup time for STOP condition	tSTO	1.0	-	us	

## 5.17 Electrical Characteristics for SPDIF Transmitter

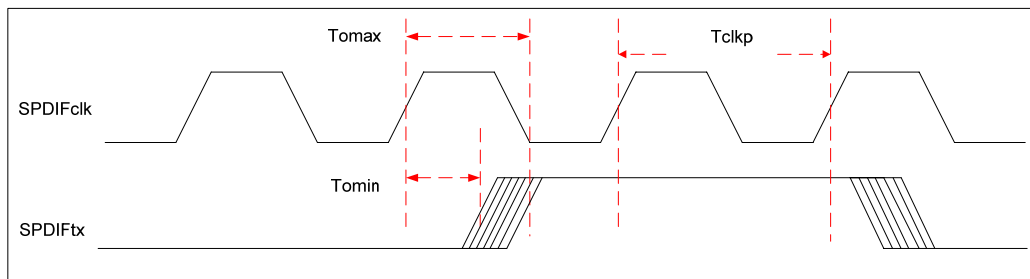


Figure 5.10 Timing Diagram for SPDIF Transmitter

Table 5.26 Timing Parameters for Each Symbol

Parameter	Symbol	Min	Max	Unit	Remark
SPDIFclk Clock Cycle Time	Tclkp	110		ns	
SPDIFclk Data Output Time Referenced to SPDIFclk	Tomin/Tomax	1	10	ns	CL = 50pF

## 5.18 Electrical Characteristics for DAI(I2S)

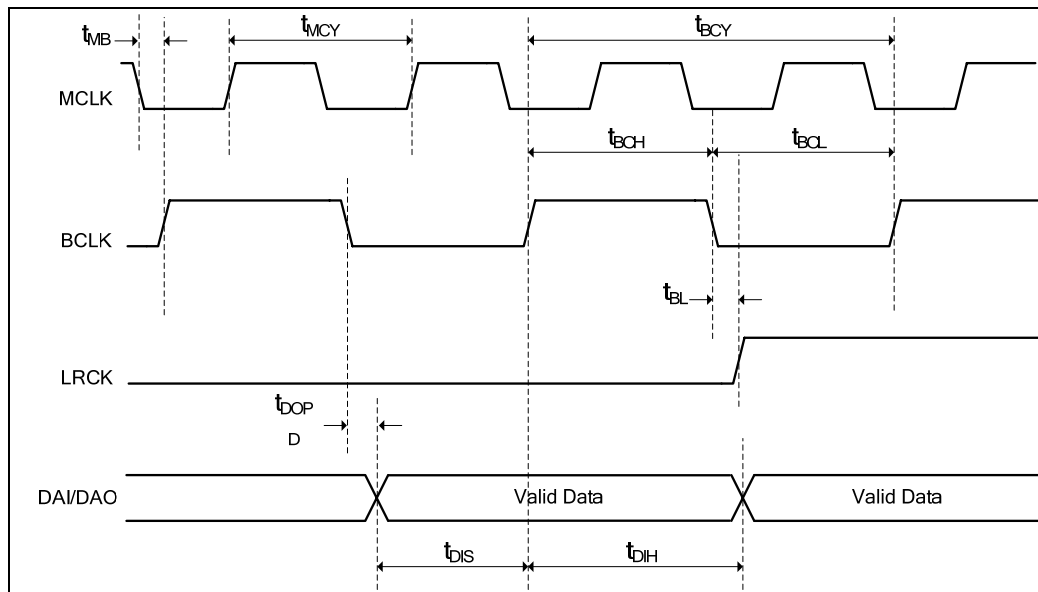


Figure 5.11 Timing Diagram for DAI (receiver)

Test Conditions

MODE = I2S,  $f_s = 48\text{KHz}$ , MCLK = 256fs, BCLK = 64fs

Table 5.27 Timing for DAI (receiver)

Parameter	Symbol	Min	Typ	Max	Unit	Remark
MCLK cycle time	$t_{MCY}$	19.40	81.40		ns	
BCLK cycle time	$t_{BCY}$	$4 * t_{MCY}$	$4 * t_{MCY}$		ns	
BCLK pulse width high	$t_{BCH}$	39	163		ns	
BCLK pulse width low	$t_{BCL}$	38	162		ns	
MCLK to BCLK	$t_{MB}$	0.18	0.18		ns	
BCLK to LRCK	$t_{BL}$	14.77	14.77		ns	
DAI setup time to BCLK rising edge	$t_{DIS}$	1	1		ns	
DAI hold time from BCLK rising edge	$t_{DIH}$	1	1		ns	
DAO Output Timing Referenced to BCLK	$t_{DOPD}$			1	ns	

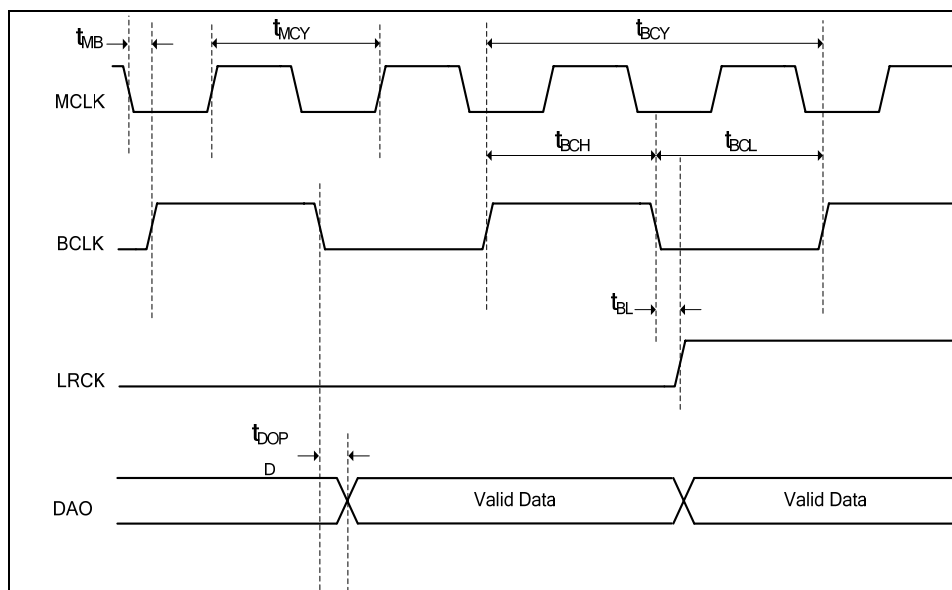


Figure 5.12 Timing Diagram for DAI Transmitter

Table 5.28 Timing Parameters for Each Symbols

Parameter	Symbol	Min	Max	Unit	Remark
MCLK cycle time	$t_{MCY}$	36		ns	
BCLK cycle time	$t_{BCY}$	$16 * t_{MCY}$		ns	
BCLK pulse width high	$t_{BCH}$	$8 * t_{MCY}$		ns	
BCLK pulse width low	$t_{BCL}$	$8 * t_{MCY}$		ns	
MCLK to BCLK	$t_{MB}$	19		ns	
BCLK to LRCK	$t_{BL}$	13		ns	
DAO Output Timing Referenced to BCLK	$t_{DOPD}$	1		ns	



## 5.19 Electrical Characteristics for Nand Flash Controller

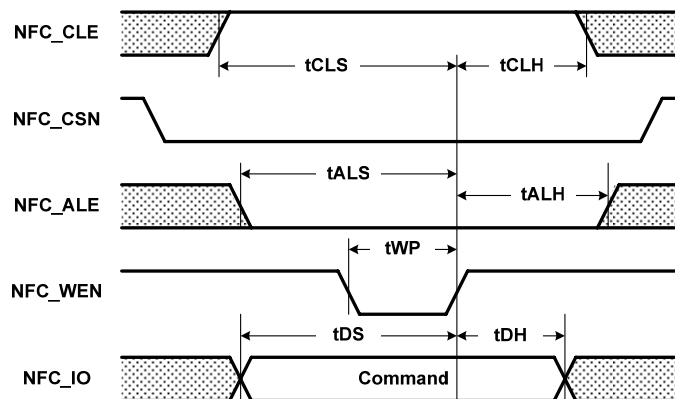


Figure 5.13 Timing Diagram for Command Latch Enable Cycle

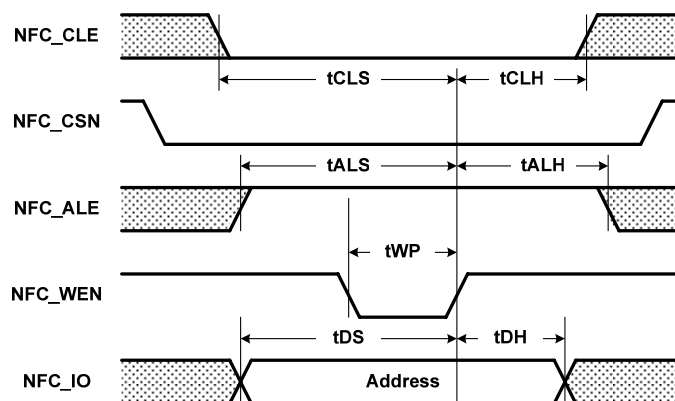


Figure 5.14 Timing Diagram for Single Address Latch Cycle

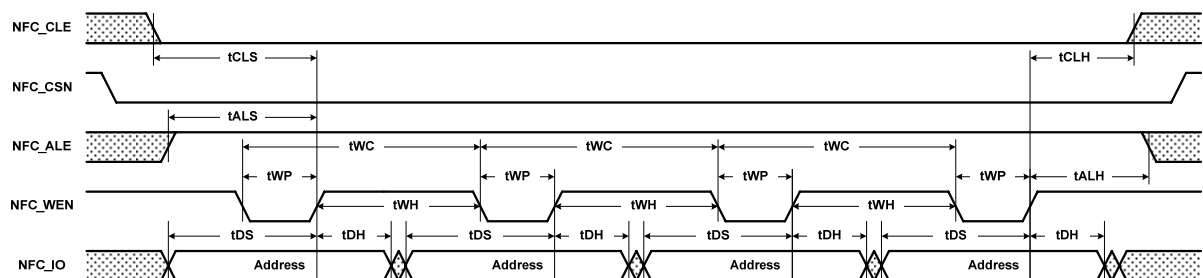


Figure 5.15 Timing Diagram for Linear Address Latch Cycle

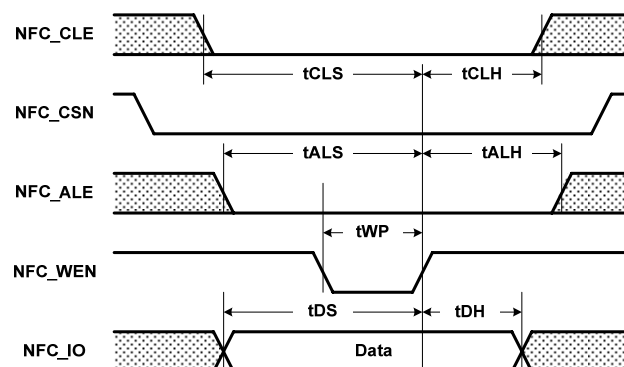


Figure 5.16 Timing Diagram for Single Data Write Cycle

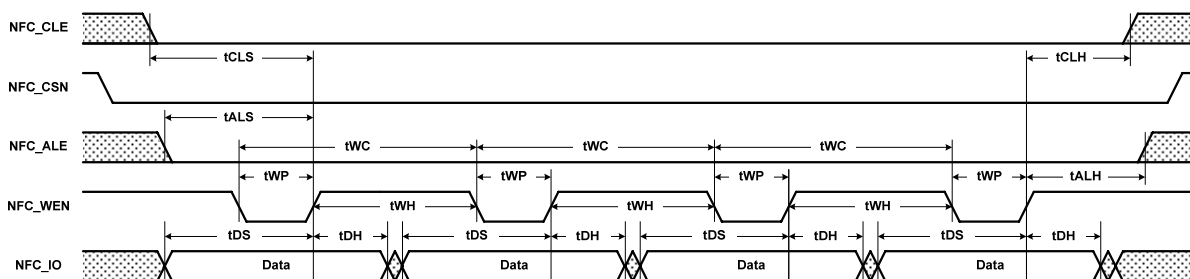


Figure 5.17 Timing Diagram for Linear Data Write Cycle

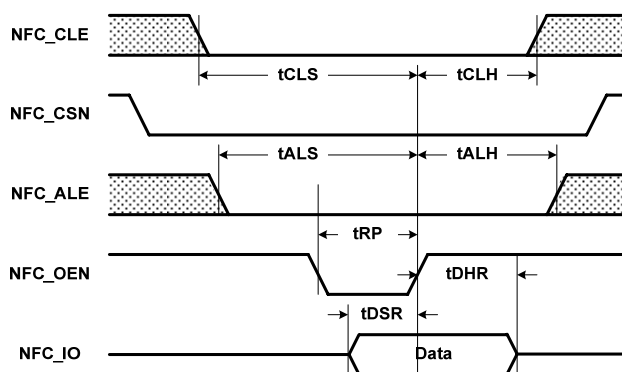


Figure 5.18 Timing Diagram for Single Data Read Cycle

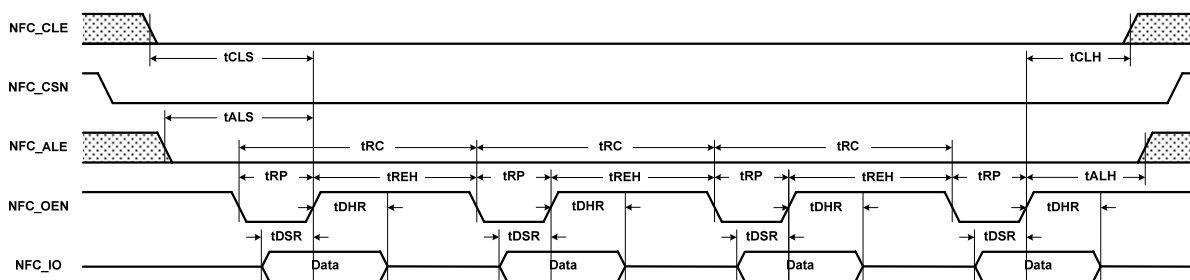


Figure 5.19 Timing Diagram for Linear Data Read Cycle

Table 5.29 Timing Parameters for Each Symbol

Parameter	Symbol	Min	Max	Unit
Clock Period	tHCLK	10		ns
CLE Set-Up Time	tCLS	$(STP + PW) \times tHCLK + 1.0$	$(STP + PW) \times tHCLK + 2$	ns
CLE Hold Time	tCLH	$HLD \times tHCLK - 2.0$	$HLD \times tHCLK - 1.0$	ns
WEN Pulse Width	tWP	$PW \times tHCLK$	$PW \times tHCLK$	ns
WEN High Hold Time	tWH	$(STP + HLD) \times tHCLK$	$(STP + HLD) \times tHCLK$	ns
Write Cycle Time	tWC	$(STP + PW + HLD) \times tHCLK$	$(STP + PW + HLD) \times tHCLK$	ns
OEN Pulse Width	tRP	$PW \times tHCLK$	$PW \times tHCLK$	ns
OEN High Hold Time	tREH	$(STP + HLD) \times tHCLK$	$(STP + HLD) \times tHCLK$	ns
Read Cycle Time	tRC	$(STP + PW + HLD) \times tHCLK$	$(STP + PW + HLD) \times tHCLK$	ns
ALE Set-Up Time	tALS	$(STP + PW) \times tHCLK - 1.00$	$(STP + PW) \times tHCLK + 2.00$	ns
ALE Hold Time	tALH	$HLD \times tHCLK - 2.00$	$HLD \times tHCLK + 1.00$	ns
Data Set-Up Time	tDS	$(STP + PW) \times tHCLK - 7.00$	$(STP + PW) \times tHCLK - 1.00$	ns
Data Hold Time	tDH	$HLD \times tHCLK - 1.00$	$HLD \times tHCLK + 1.00$	ns
Data Set-Up Time in READ	tDSR	5.00	15.0	ns
Data Hold Time in READ	tDHR	0	0	ns

Table 5.30 I/O Function Name for Corresponding Signal Name

Signal Name	I/O Function Name
NFC_CSN	NAND_CSN0, NAND_CSN1
NFC_ALE	NAND_ALE
NFC_CLE	NAND_CLE
NFC_OEN	NAND_OEN
NFC_WEN	NAND_WEN
NFC_IO[15:0]	NANDXD[15:0]

## 5.20 Electrical Characteristics for UART Controller

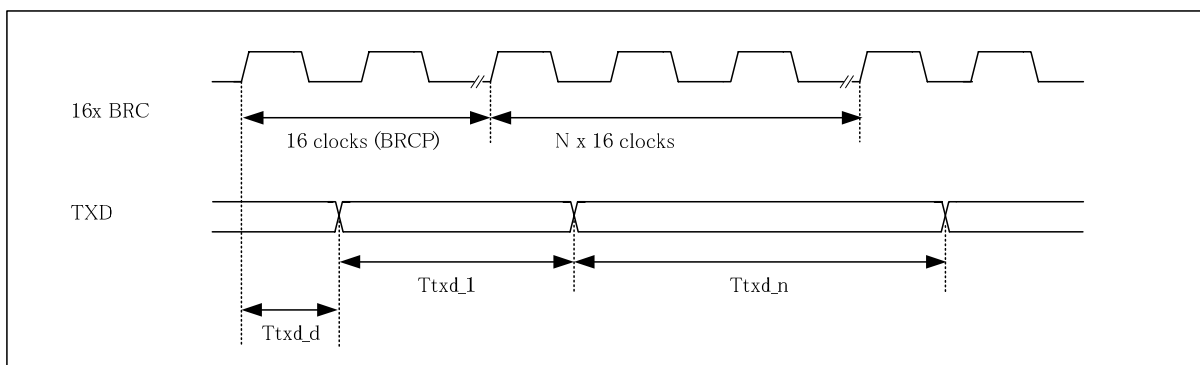


Figure 5.20 Timing Diagram for TXD

Table 5.31 Timing Parameters for Each Symbol

Parameter	Symbol	Min	Max	Unit	Remark
Pulse duration of 1bit TXD	Ttxd_1	BRCP -15	BRCP +15	ns	3.3V
Pulse duration of nbit TXD	Ttxd_n	N x BRCP -15	N x BRCP + 15	ns	3.3V
TXD output delay time	Ttxd_d	0.5	15	ns	3.3V

- BRC : Baud-Rate Clock
- BRCP : Baud-Rate Clock Period
- CL : 71pF

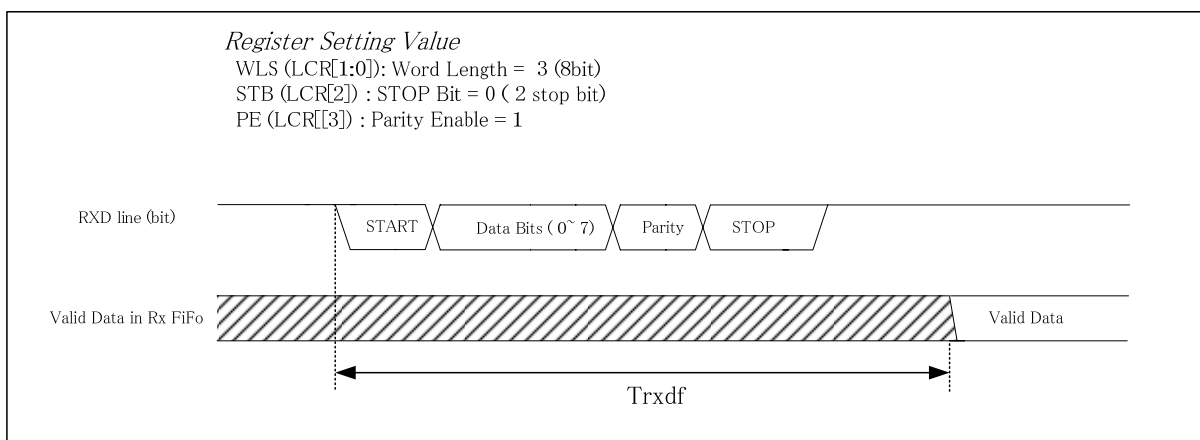


Figure 5.21 Timing Diagram for RXD

Table 5.32 Timing Parameters for Each Symbol

Parameter	Symbol	Min	Max	Unit	Remark
RXD Start to Rx FiFo.	Trxdf	10.5 x BRCP	11 x BRCP	ns	3.3V

- BRC : Baud-Rate Clock
- BRCP : Baud-Rate Clock Period
- CL : 71pF

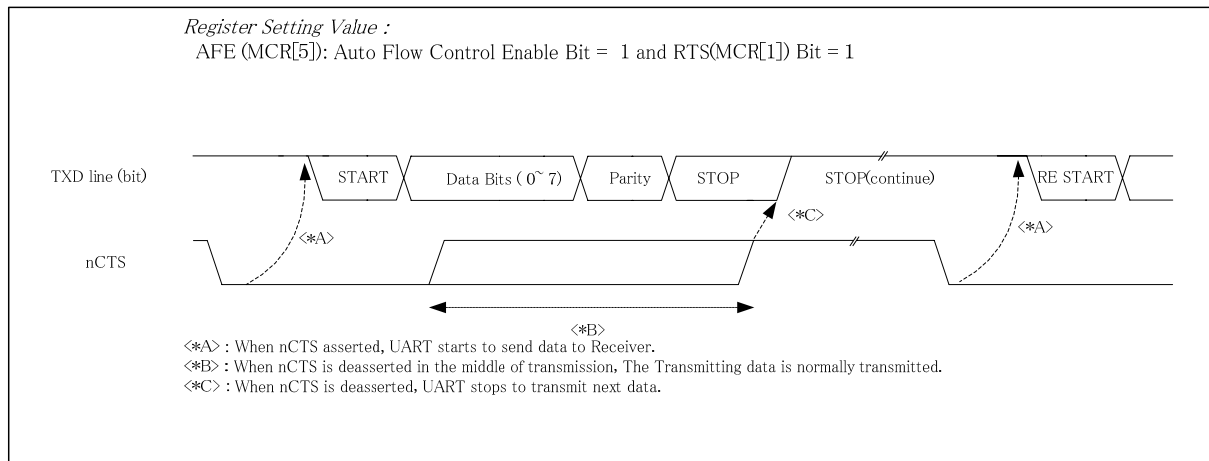


Figure 5.22 Timing Diagram for TX Operation with H/W Flow Control

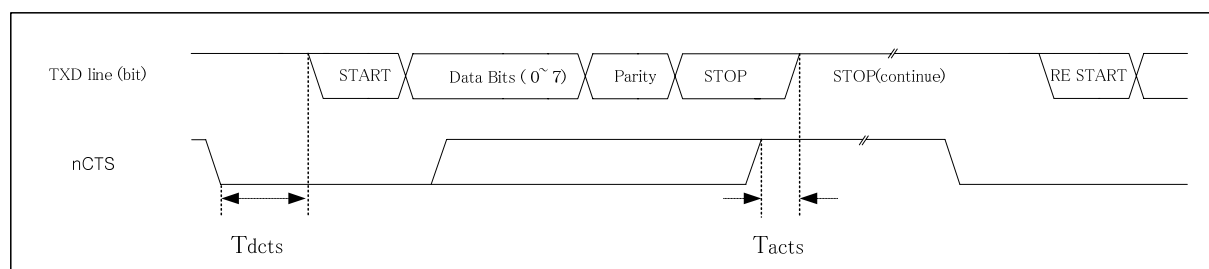


Figure 5.23 Timing Diagram for nCTS Timing Diagram

Table 5.33 Timing Parameters for Each Symbol

Parameter	Symbol	Min	Max	Unit	Remark
Deasserted nCTS to Tx Start	Tdcts	-	BRCP	ns	3.3V
Deasserted nCTS to Tx Stop :to stop next transmission(setup time)	Tacts	4 x BRCP/16	-	ns	3.3V

● BRC : Baud-Rate Clock , BRCP : Baud-Rate Clock Period , CL : 71pF

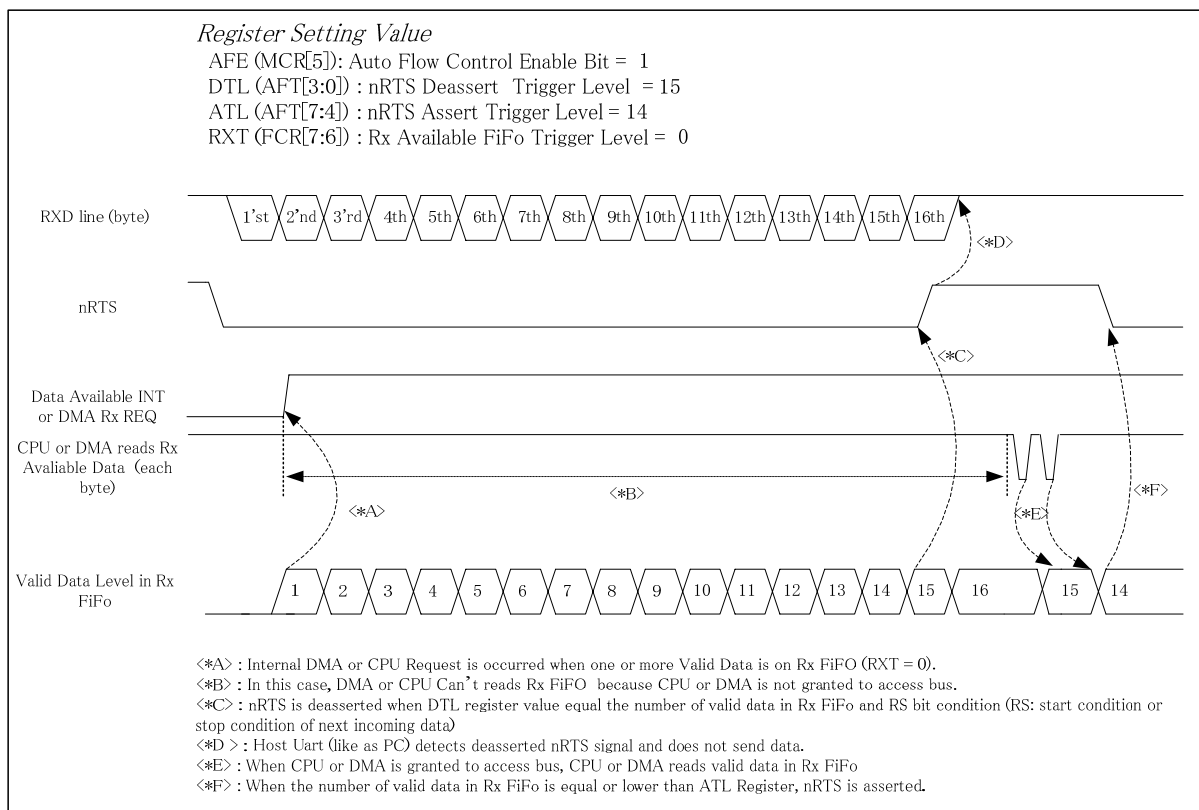


Figure 5.24 Timing Diagram for RX Operation with H/W Flow Control

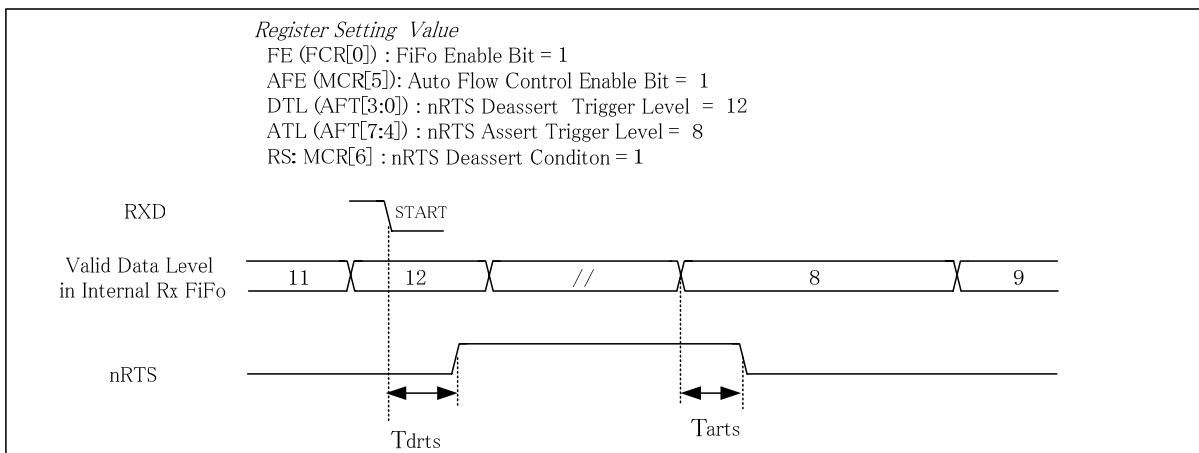


Figure 5.25 Timing Diagram for nRTS Timing Diagram

Table 5.34 Timing Parameters for Each Symbols

Parameter	Symbol	Min	Max	Unit	Remark
DTL(and RXD start condition) to deasserted nRTS	Tdrtts	-	BRCP	ns	3.3V
ATL to asserted nRTS	Tarts	-	BRCP/16 + 8	ns	3.3V

● BRC : Baud-Rate Clock , BRCP : Baud-Rate Clock Period , CL : 71pF